

# Compal Confidential

## A940 Schematics Document

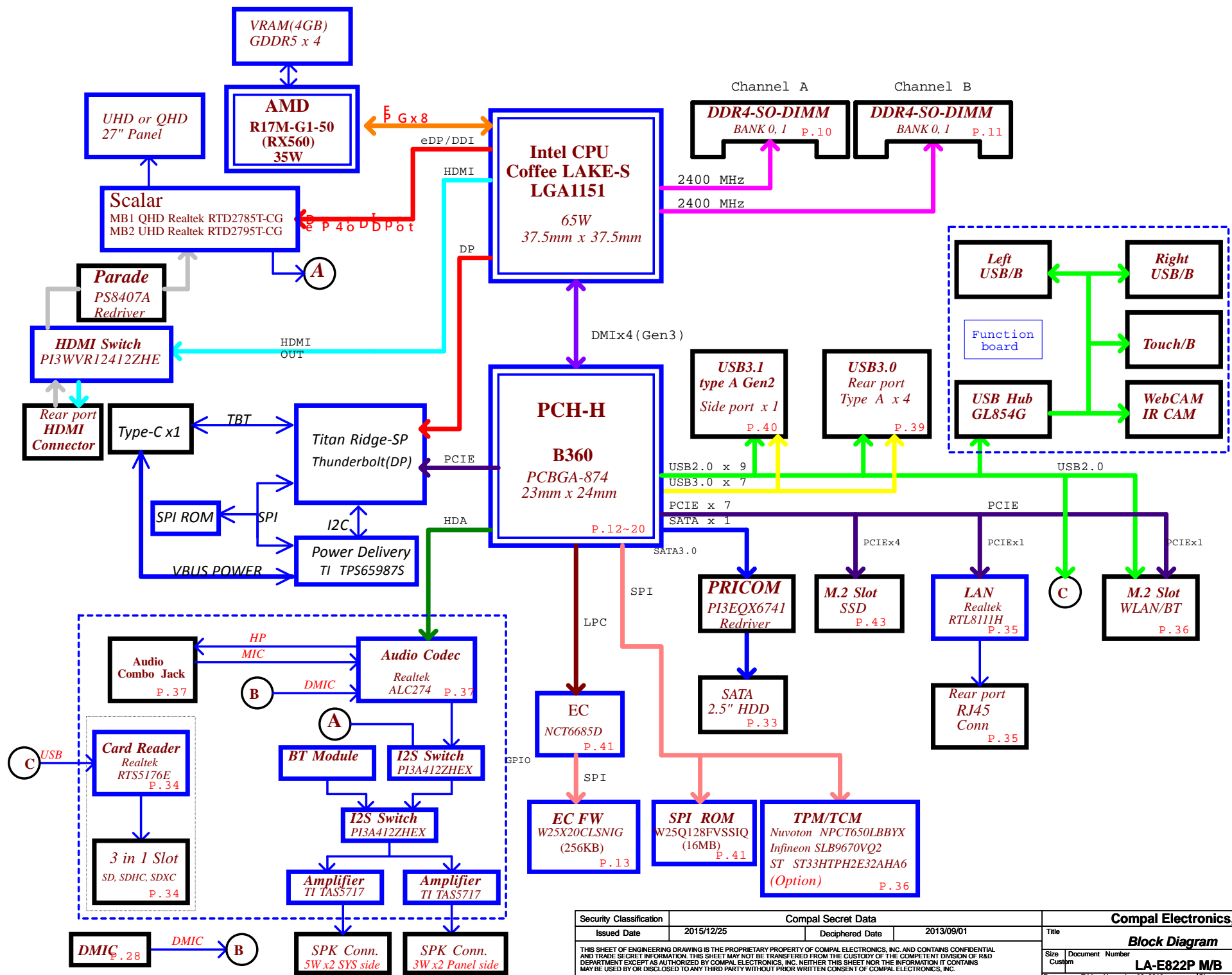
INTEL Coffeelake-S CPU with DDR4 + AMD GPU(R17M-G1-50)

AIO M/B

10/31 , 2018

REV : 1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2015/12/25	Deciphered Date	2013/09/01	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Title		Cover Page	
		Size	Document Number	Rev	
		Custom	LA-E822P M/B	0.1	
		Date:	Friday, November 02, 2018	Sheet	1 of 73



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Block Diagram		
				Size	Document Number	Rev
				Custom	LA-E822P M/B	0.1
				Date:	Friday, November 02, 2018	Sheet 2 of 73

PCIe Port Table		
No.	Port	Device
6	12	LAN
7	13	WLAN
17	23	TBT
18	24	TBT
19	25	TBT
20	26	TBT
21	27	SSD
22	28	SSD
23	29	SSD
24	30	SSD

SATA Port Table		
No.	Port	Device
0	19	HDD
1	20	
2	21	
3	22	
4	23	
5	24	

DDI Port Table		
No.	Port	Device
1	DDI1	HDMI OUT
2	DDI2	TBT
3	DDI3	NC

USB2.0 Port Table		
Port	Device	OC#
1	USB3.1 Gen1 Rear IO Port 1	OC#0
2	USB3.1 Gen1 Rear IO Port 2	OC#1
3	USB3.1 Gen1 Rear IO Port 3	OC#2
4	USB3.1 Gen1 Rear IO Port 4	OC#3
5	USB3.1 Gen1 SIDE IO TYPE-C	NA
6	USB3.1 Gen2 SIDE IO TYPE-A	OC#4
7	TO SB Board	NA
8	Card Reader	NA
9	TBT_PD	NA
10	NC	NA

BOARD ID Table	
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	

USB3.0 Port Table		
No.	Port	Device
1	1	USB3.0 (Rear IO)
2	2	USB3.0 (IO Board Port 1)
3	3	NC
4	4	NC
5	5	USB3.0 (IO Board Port 2)
6	6	NC

BOM Structure Table	
BOM Structure	BTO Item
B Z	A D 8 2 2 8 L 8 8 P C
@ a h @ x x x	U 8 p
f @	f 1 p b h
M T	M I 8 p p m o e t
@ M @	M I 8 p p m o e t
F D	F D 8 p p m o e t
@ S @	F D 8 p p m o e t
D T	G H
V G S	V M r 1 5 m y h c o f g
V G M	V M r 1 5 m y h c o f g
V G M N	V M r 1 5 m y h c o f g
M O	G A Y B o t M B
N M	V A N s u p t m b
W H	W F P S C R P e s p b t
T M	H T M
W T M	O H T M
M B	Y S S M s u p t m b
N S B	Y S S M n o s p b t m b

Voltage Rails		S0	S3	S4/S5
Power Plane	Description			
+DC20V	AC or battery power rail for power circuit.	N/A	N/A	N/A
+RTCVCC_S5	RTC power	ON	ON	ON*
+3V3_DS_W	3.3V DS_W on power rail	ON	ON	ON*
+3VALW_S5	3.3V always on power rail	ON	ON	ON
+5VALW_S5	5V always on power rail	ON	ON	ON
+12VALW_S5	12V always on power rail	ON	ON	ON
+1.8VS_S0	1.8V always on power rail	ON	OFF	OFF
+1.0VALW_S5	1.0V always on power rail	ON	ON	ON
+1.0V_VCCST_S3	1.0V power rail for CPU VCCST	ON	ON	OFF
+1.2V_VDDQ_S3	1.2V power rail for DDR4	ON	ON	OFF
+2.5V_S3	2.5V power rail for DDR4	ON	ON	OFF
+CPU_VCCIO_S0	0.95V power rail for CPU VCCIO	ON	OFF	OFF
+5VS_S0	5V switched power rail	ON	OFF	OFF
+3VS_S0	3.3V switched power rail	ON	OFF	OFF
+12VS_S0	12V switched power rail	ON	OFF	OFF
+1.05VS_S0	+1.5VS on power rail for CPU VCCSA	ON	OFF	OFF
+CPU_CORE	VCC Core voltage for CPU	ON	OFF	OFF
+VCC_GT_S0	Core voltage for CPU graphic	ON	OFF	OFF
+3VS_DGPU_S0	3.3V power rail for DIS graphic	ON	OFF	OFF
+VGA_CORE_S0	VCC Core voltage for GPU	ON	OFF	OFF
+1.05VS_DGPU_S0	1.05V power rail for DIS graphic	ON	OFF	OFF
+1.35VS_VGA_S0	1.35V power rail for VRAM	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

SKU ID(Project) Table

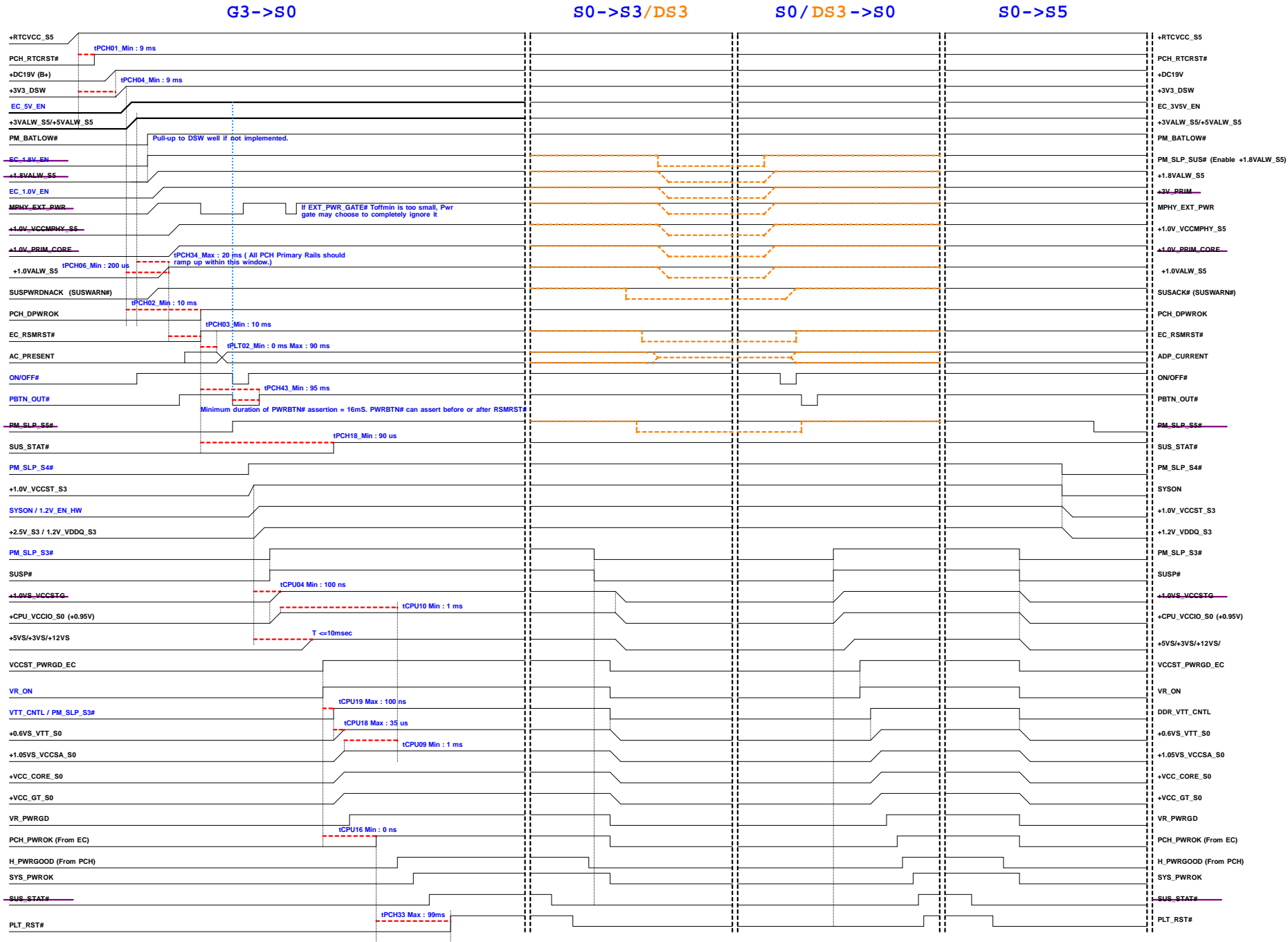
SKU (Only DIS)	C7 DVT UHD BOM Configure Table
431ADT38L01 HYNIX 4G (DIS)	A Z U D b S M W N M O W H @ A N @ W T M @ R @
431ADT38L02 MICRON 4G (DIS)	A Z U D b S M B N M O W H @ A N @ W T M @ R @
431ADT38L03 MICRON 4G (DIS)	A Z U D b S B @ M O @ H G A N @ W T M @ R @
X4EADT38L01	M P S B S K E I M @
X7679238L01 SAMSUNG 4G	V G S SAMSUNG - SA000092D10 S IC D5 256M32 K4G80325FB-HC28 FBGA 170P
X7679238L02 HYNIX 4G	V G H HYNIX - SA00009U150 S IC D5 256M32 H5GC8H24AJR-R0C BGA 170P
X7679238L03 MICRON 4G	V G M MICRON - SA00009TV60 S IC D5 256M32 MT51J256M32HF-70:B FBGA

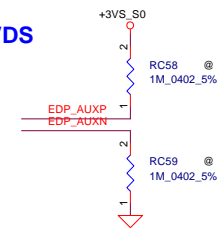
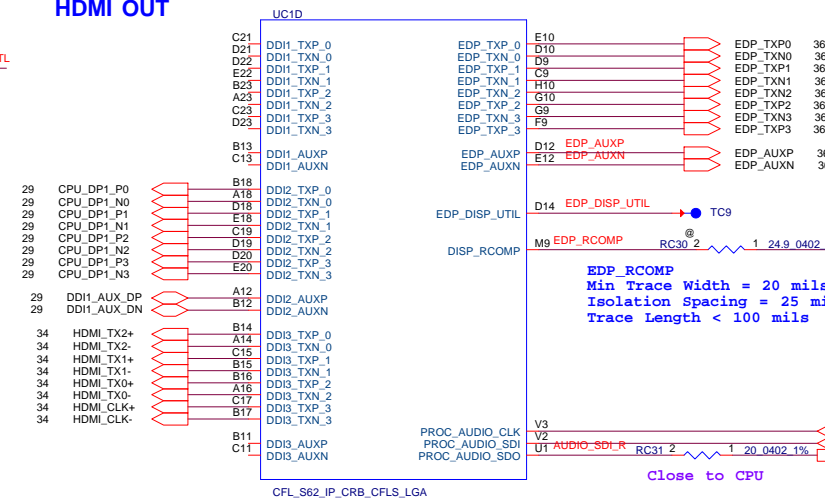
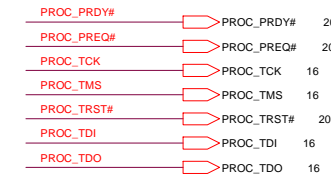
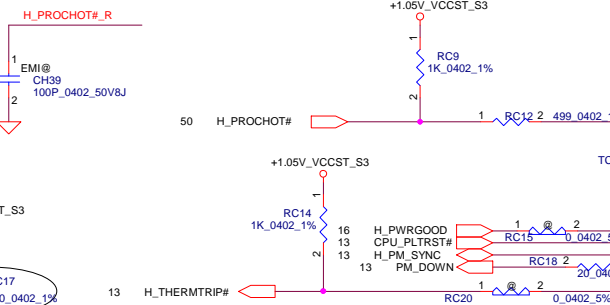
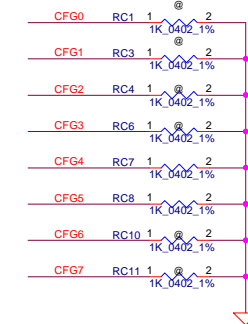
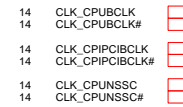
EC SM Bus0 Address		
Device	Address	HEX
Converter RTD-2136N	0110-0010xb	62
GPU	1001-1110xb	9E

EC SM Bus2 Address		
Device	Address	HEX
Scalar RTD-2506S	1001-0100xb	94
LCD Backlight		

PCH SM Bus Address		
Device	Address	HEX
DDR(JDIMM1)	WRITE:0xA0	READ: 0xA1
DDR(JDIMM2)	WRITE:0xA4	READ: 0xA5

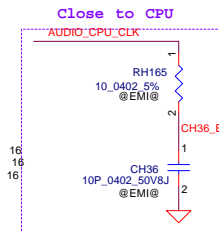
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Notes List
Size C	Document Number	LA-E881P M/B		Rev 0.1
Date:	Friday, November 02, 2018	Sheet	3 of 73	



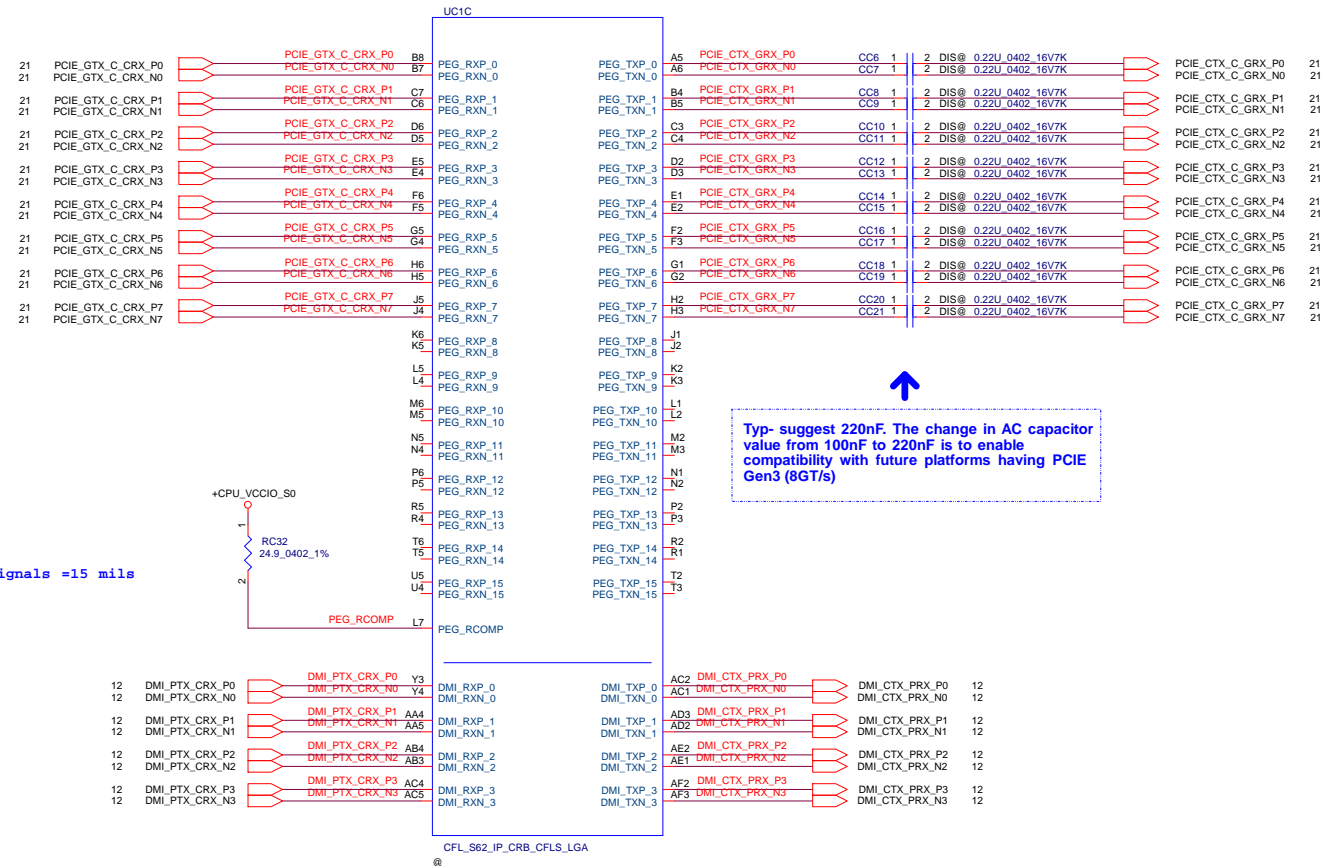


Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detected used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CLK	
	DDPB_CTRLDATA	DDI1_CTRL_DATA	

<b>Compal Electronics, Inc.</b>				
Title <b><i>Skylake JTAG/XDP/DDI</i></b>				
Size Custom	Document Number	LA-F901P M/B		Rev 0.1
Date:	Friday, November 02, 2018	Sheet	5 of 73	

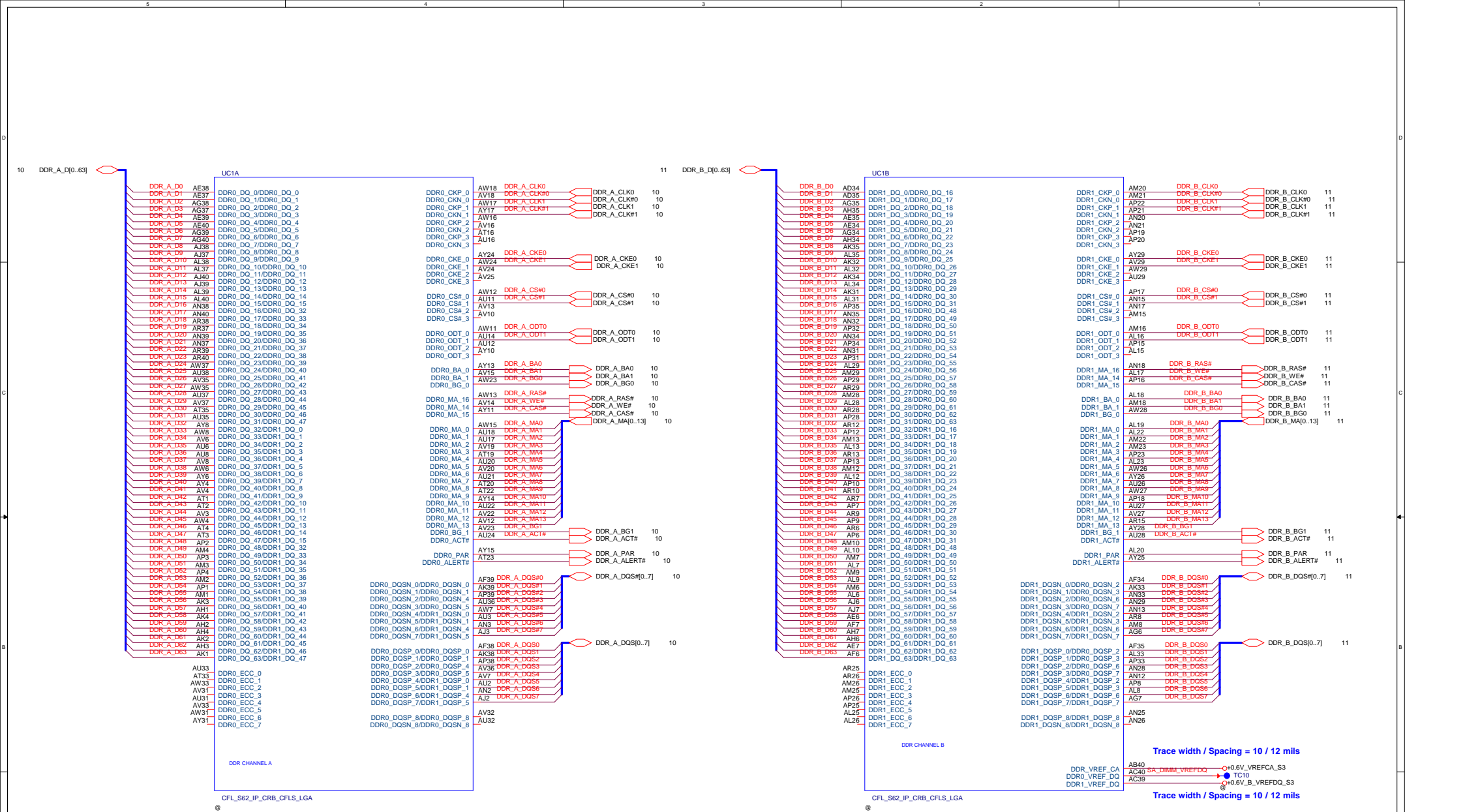


PEG\_RCOMP  
Trace Width = 5 mils  
Trace Spacing to Other Signals =15 mils  
Trace Length < 600 mils



Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/01	Deciphered Date	2013/09/01	Title	Skylake DMI/PEG/FDI
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Document Number	Rev
				Custom	0.1
				Date: Friday, November 02, 2018	Sheet 6 of 73



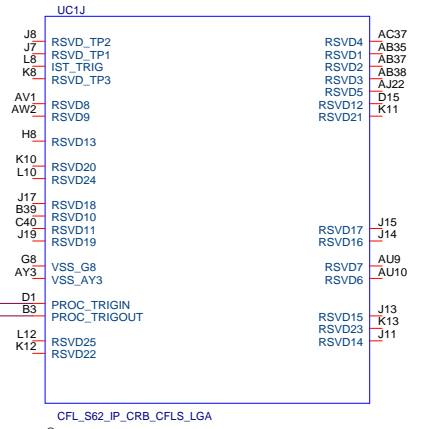
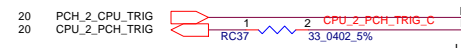
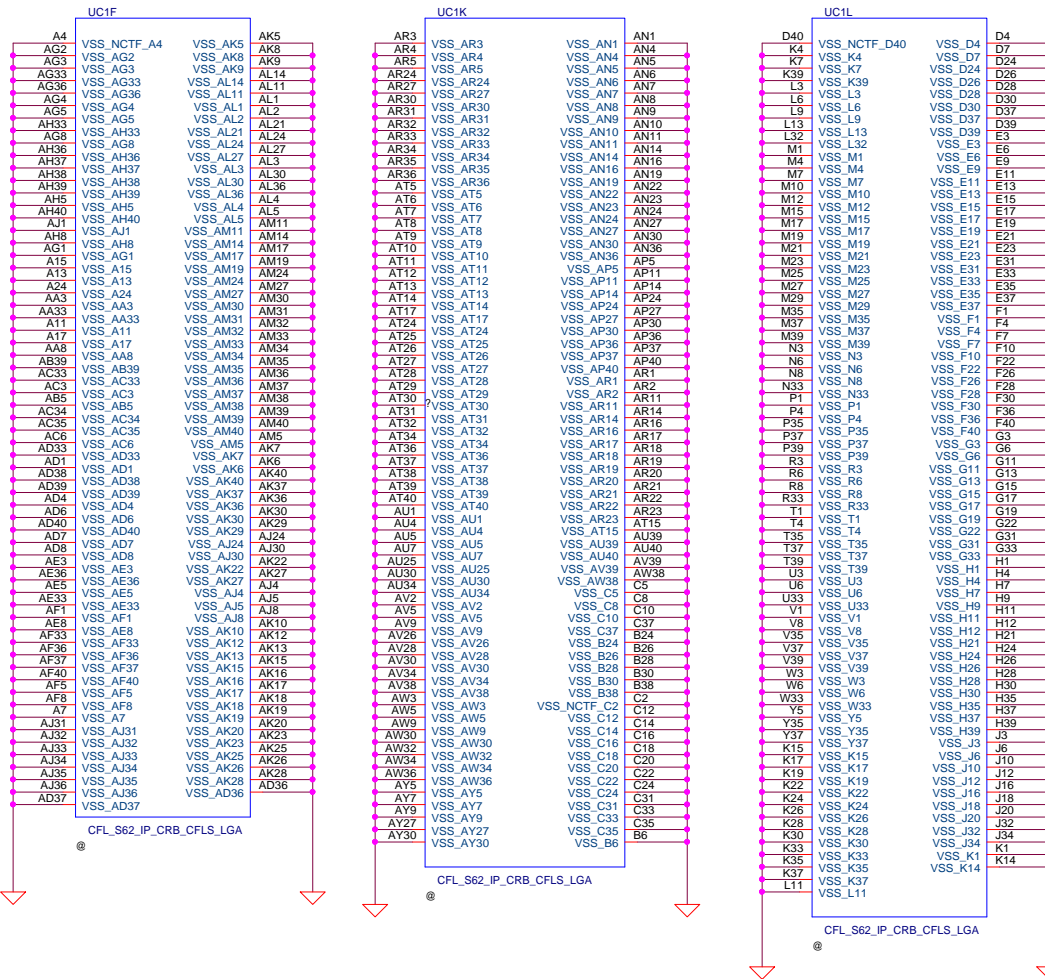
www.teknisi-indonesia.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title	Skylake DDR4
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-F901P M/B
				Date	Friday, November 02, 2016
				Sheet	7 of 73
				Rev	0.1



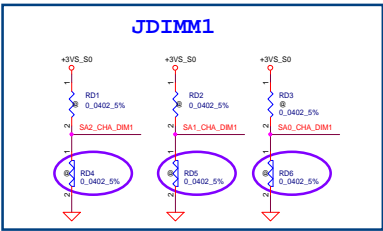






Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2015/12/25		Deciphered Date		2013/09/01		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Skylake GND/RSVD					
						Size		Document Number		Rev	
						Custom		LA-F901P M/B		0.1	
Date:		Friday, November 02, 2018		Sheet		9		of 73			

INTERLEAVE  
CHANNEL-A

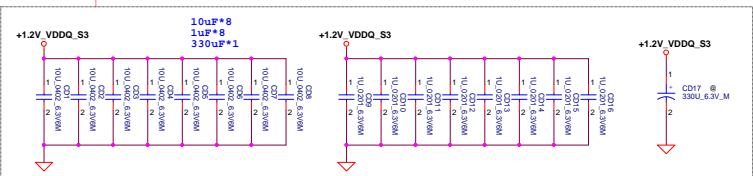


PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

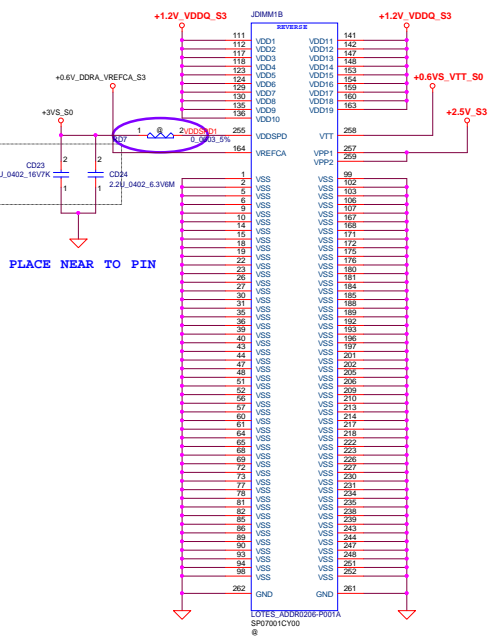
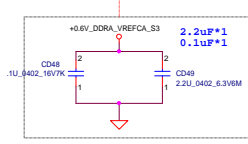
(4.0 mm) Reverse Type

SPD ADDRESS FOR CHANNEL A :  
WRITE ADDRESS: 0xA0  
READ ADDRESS: 0xA1  
SA0 = 0; SA1 = 0; SA2 = 0.  
DDR4 POR OPERATING SPEED: 1867 MT/S  
STRETCH GOAL IS 2133 MT/S

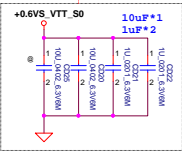
Layout Note:  
Place near JDIMM1



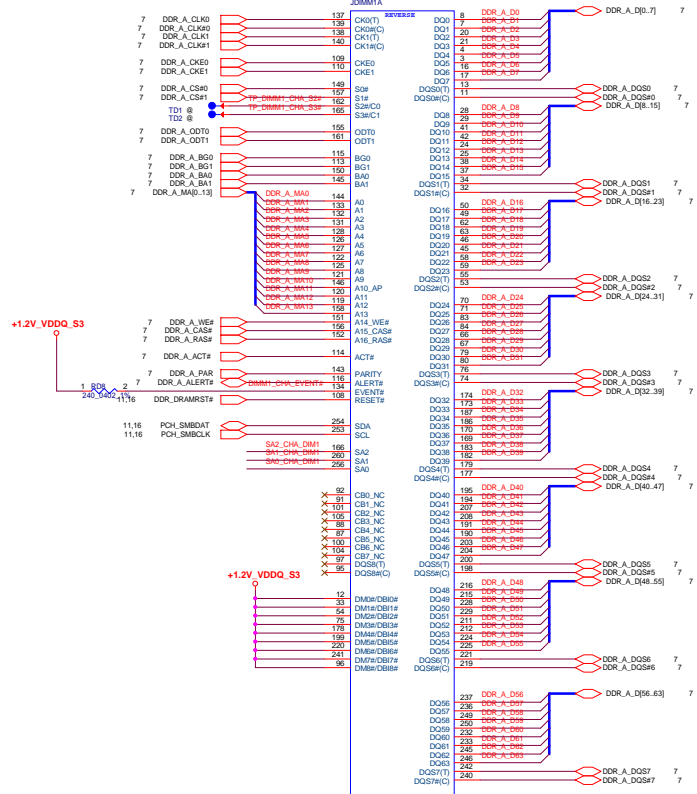
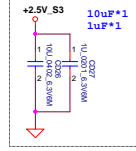
Layout Note:  
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM1



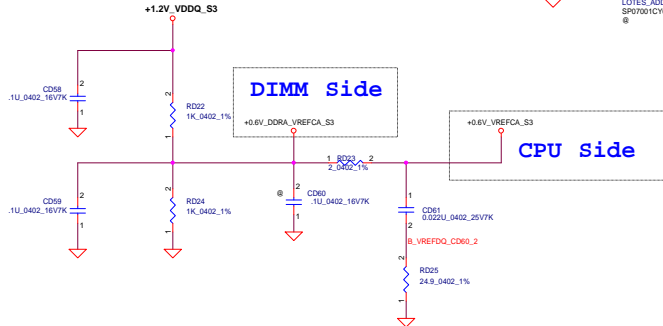
Layout Note:  
Place near JDIMM1



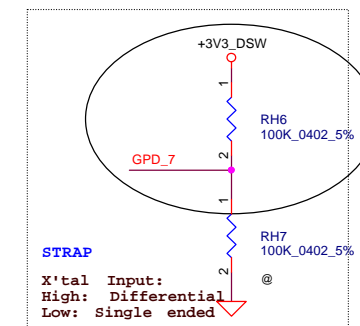
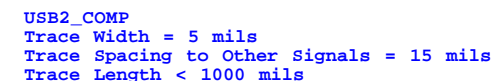
Layout Note:  
Place near JDIMM1



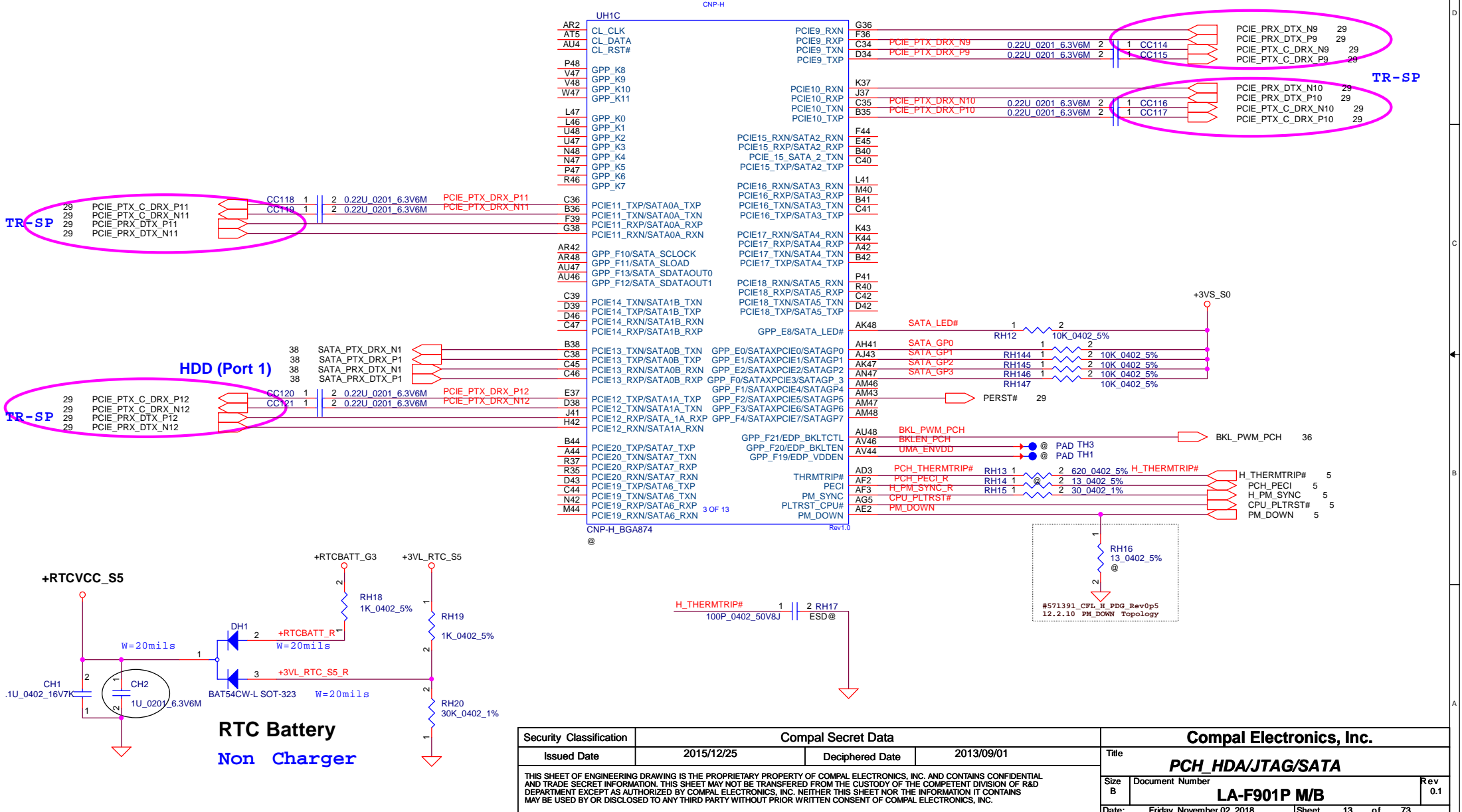
LOTES\_ADDR0209-P001A  
SP07001CY00





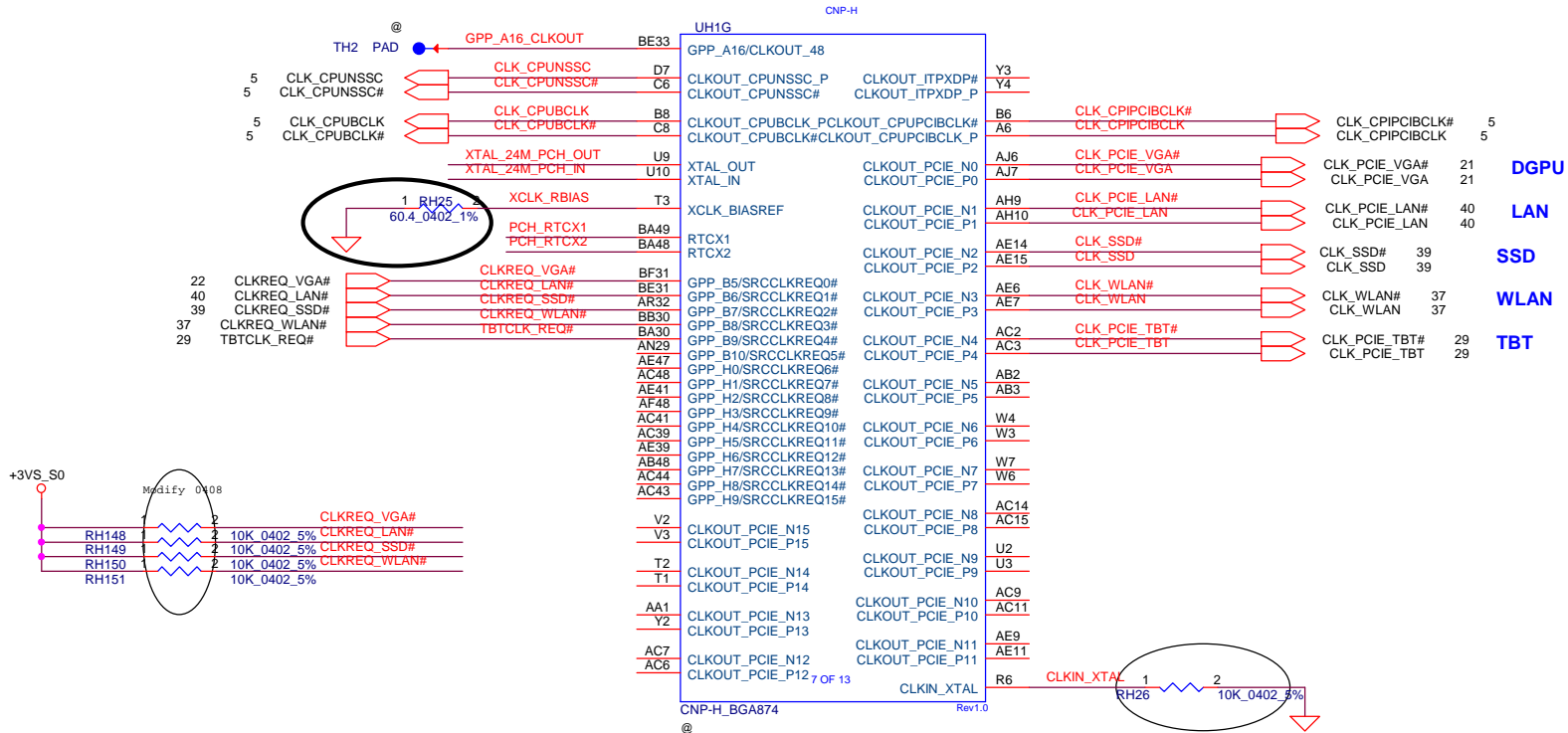
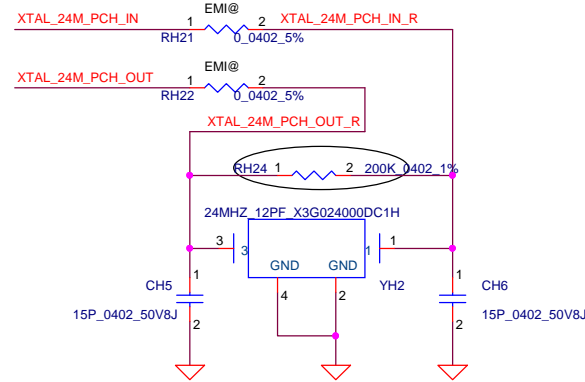
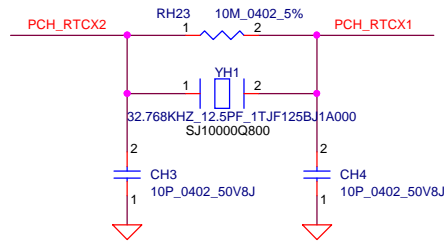


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title <b>PCH_DMI/USB2/PCIE</b>		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Document Number <b>LA-F901P M/B</b>	Rev 0.1
				Date:	Friday, November 02, 2018	Sheet 12 of 73



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PCH_HDA/JTAG/SATA	
				Size B	Document Number
				LA-F901P M/B	
Date: Friday, November 02, 2018				Sheet	13 of 73

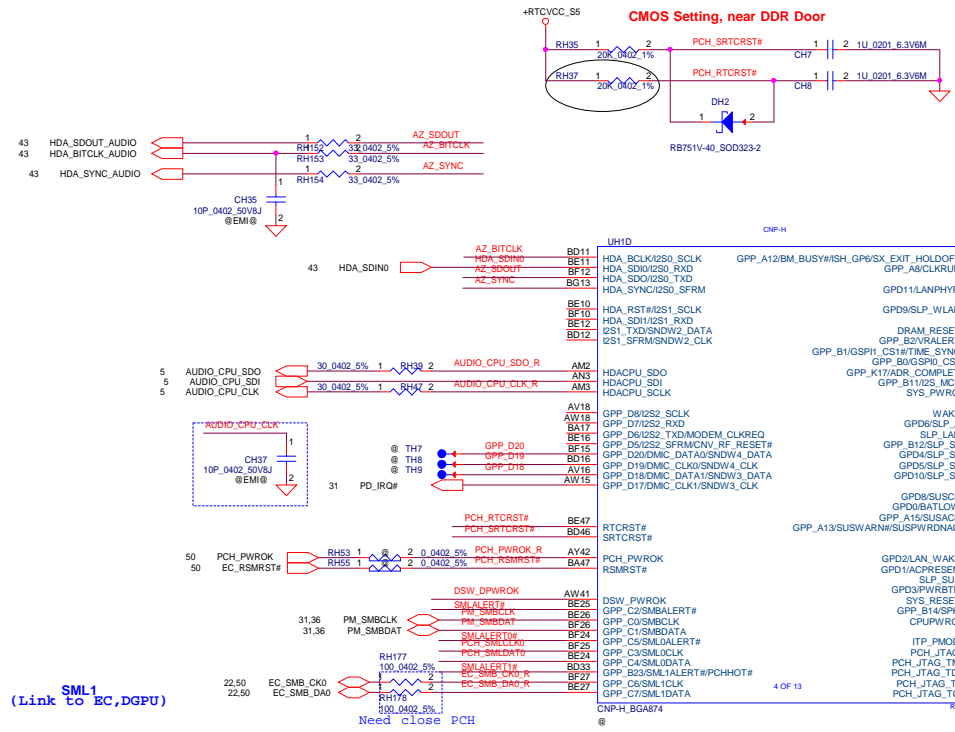
## 32.768KMHZ CRYSTAL



Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2015/12/25		Deciphered Date		2013/09/01		Title					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								PCH_CLKLPCSPISMBUS					
								Size		Document Number		Rev	
								Custom		LA-F901P M/B		0.1	
Date:				Friday, November 02, 2018		Sheet		14 of 73					



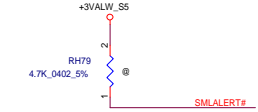




SML1  
(Link to EC,DGPU)

### Functional Strap Definitions

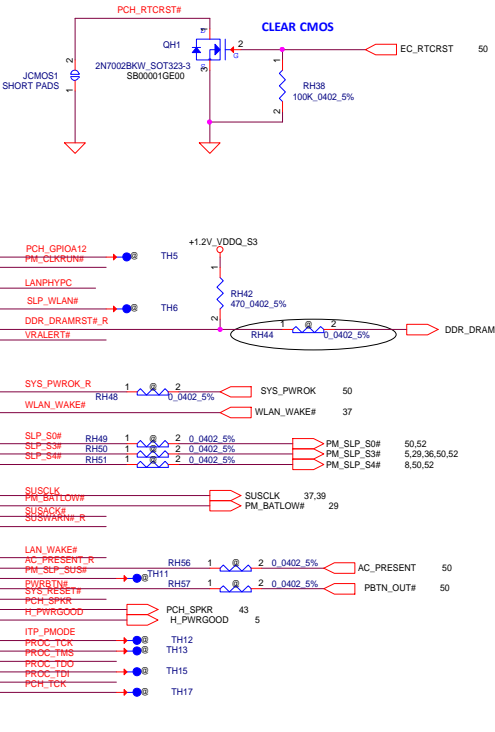
**SMLALERT#**  
This signal has a weak internal Pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.  
Notes:  
1. The internal Pull-down is disabled after RSMRST# de-asserts.  
2. This signal is in the primary well.



### Functional Strap Definitions

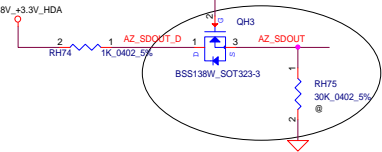
**SMLALERT0#**  
This signal has a weak internal Pull-down.  
0 = LPC is selected (for EC 9022).  
1 = eSPI is selected (for EC 9042). (Default)  
Notes:  
1. The internal Pull-down is disabled after RSMRST# de-asserts.  
2. This signal is in the primary well.

**SMLALERT1#**  
This signal has an internal pull-down.  
0 = Disable IntelR DCI-OOB (Default)  
1 = Enable IntelR DCI-OOB  
1. The internal pull-down is disabled after RSMRST# de-asserts.  
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.

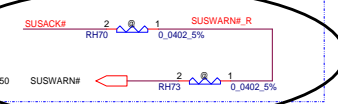
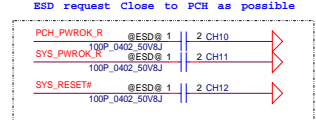
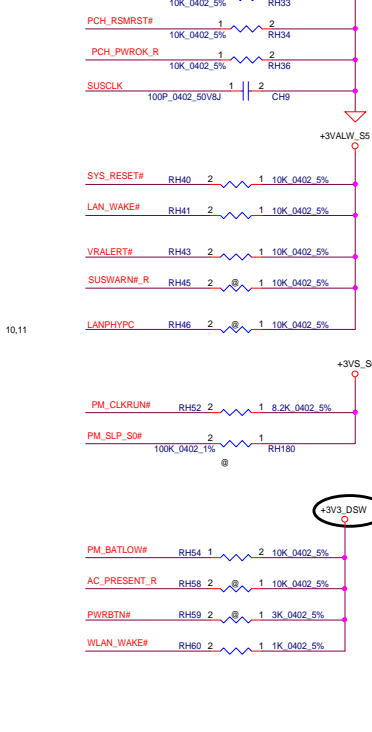


(Link to DDR)

1st source : B6S138W\_PANJIT (SB00000T000)  
2nd source : LB6S139WT1G\_LRC (SB00001GC00)  
Vgs(max)=1.5V



This signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.



Stuff RH56 if EC does not want to involve in the handshake mechanism for the DeepSx state entry and exit

### Strap Pin



Top Swap Override  
0 = Disable "Top Swap" mode (Def alt)  
1 = Enable "Top Swap" mode  
The internal Pull-down is disabled after PCH\_PWROK is high.

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2015/12/25		2013/09/01		PCH_HDAISMBUSIPM	
Size		Document Number		LA-F901P M/B	
C		Date:		Friday, November 02, 2018	
Sheet		16		of 73	

Rear GEN1

Rear GEN1

Rear GEN1

Rear GEN1

Side Gen2

+3VALW\_S5

PCH\_SPI\_SI

PCH\_SPI\_SO

PCH\_SPI\_CS#0

PCH\_SPI\_CLK

PCH\_SPI\_CS#1

PCH\_SPI\_I02

PCH\_SPI\_I03

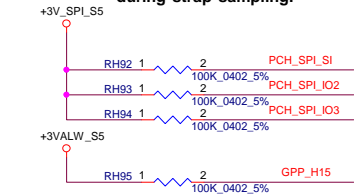
PCH\_SPI\_CS#2

TBT\_CIO\_PLUG\_EVENT#\_R1

TBT\_CIO\_PLUG\_EVENT#

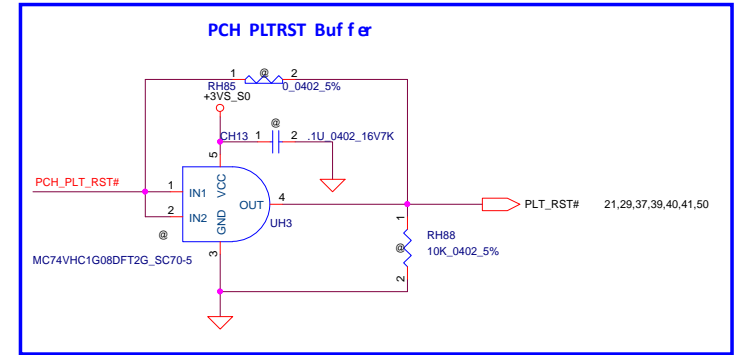
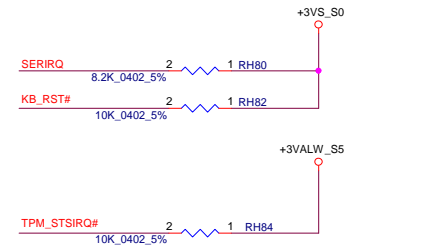
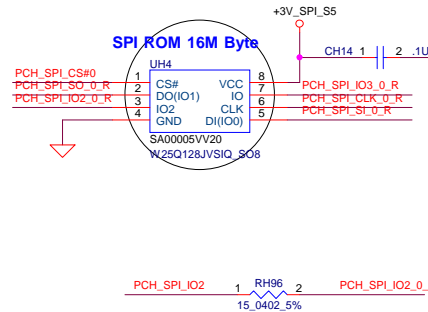
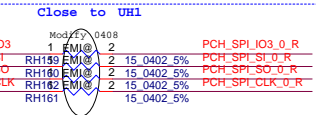
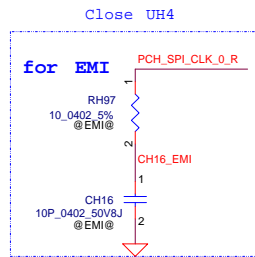
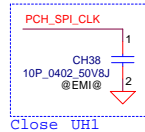
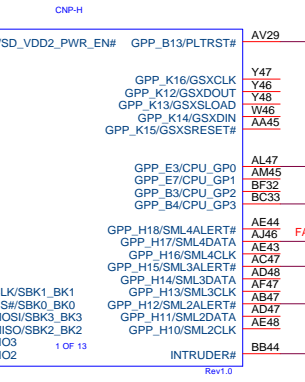
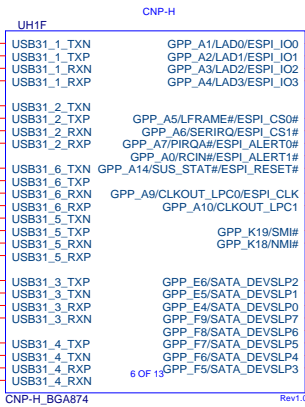
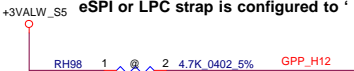
## Functional Strap Definitions

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



## Functional Strap Definitions

**SML2ALERT#**  
This signal has a weak internal pull-down.  
0 = Master Attached Flash Sharing (MAFS) enabled (Default)  
1 = Slave Attached Flash Sharing (SAFS) enabled.  
Notes:  
1. This signal is in the primary well.  
Warning: This strap must be configured to '0' if the eSPI or LPC strap is configured to '0'



www.teknisi-indonesia.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PCH_PCI-E/USB	
Size	Document Number	LA-F901P M/B		Rev	
Custom				0.1	
Date:		Friday, November 02, 2018		Sheet 17 of 73	



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PCH_POWER		
				Size B	Document Number	Rev 0.1
				LA-F901P M/B		
				Date: Friday, November 02, 2018	Sheet 19 of 73	

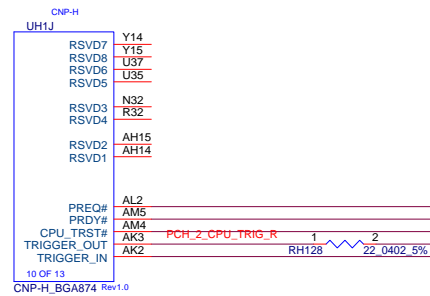
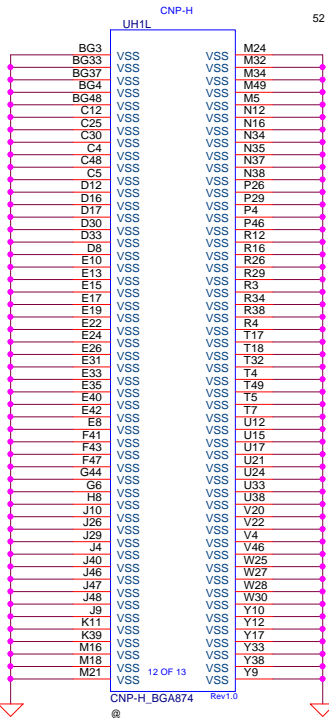
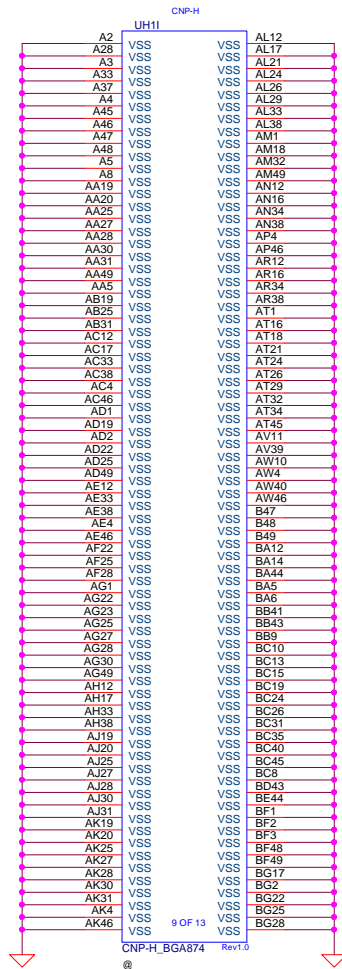
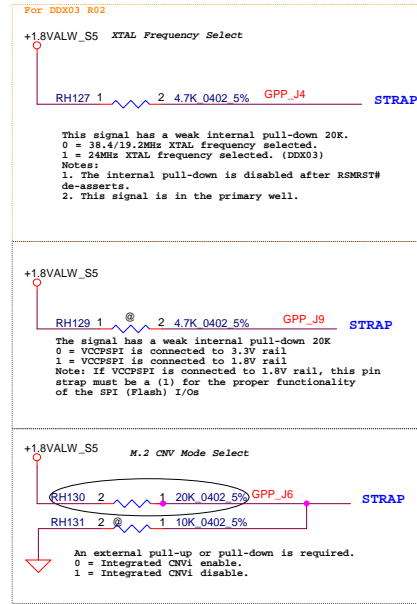
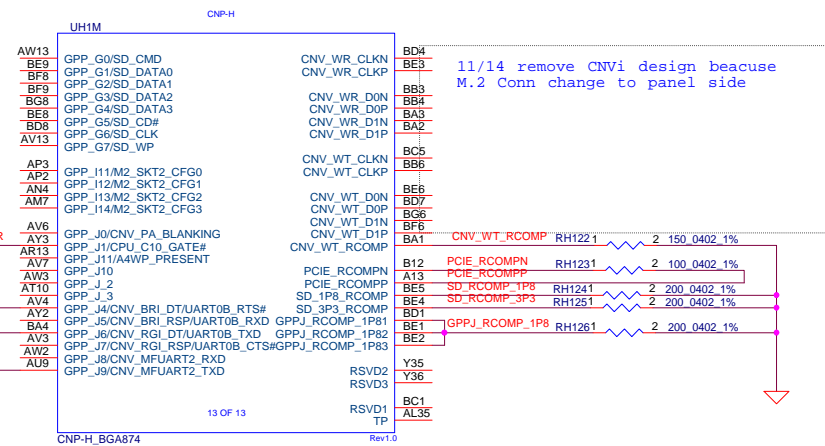


Table 18-1. GPIO Group Summary

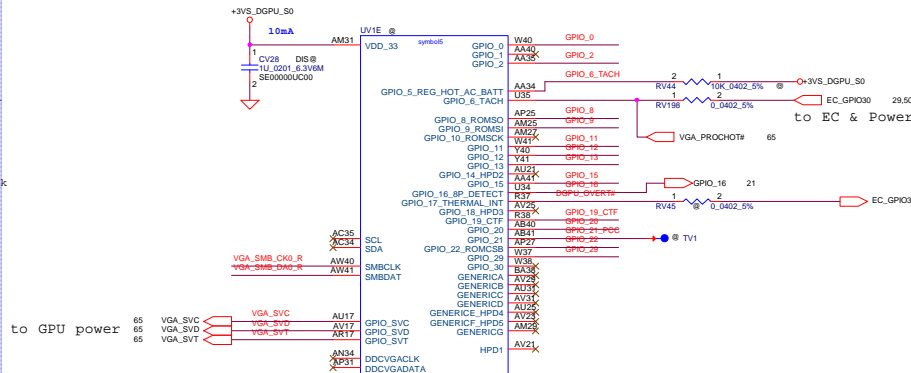
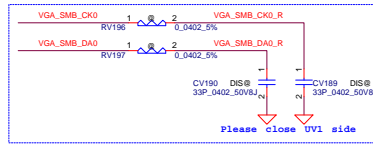
GPIO Group	Power Pins	Voltage
Primary Well Group G (GPP_G)	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8V or 3.3V
Primary Well Group H (GPP_H)	VCCPGPPHK	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCPRIM_3P3	3.3V Only
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

**Note:** Except for GPP\_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP\_G group voltage is selected by setting the corresponding soft strap only.

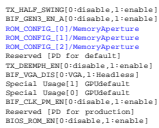
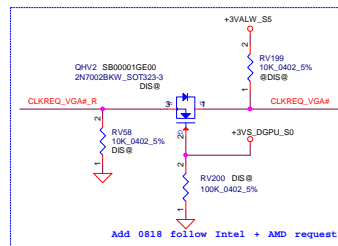
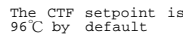








to GPU power

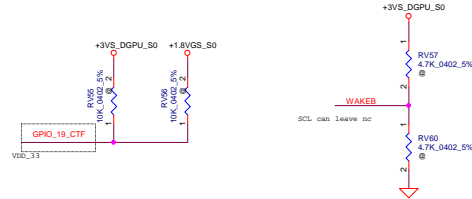
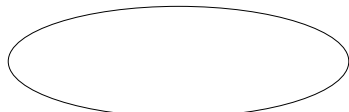


VRAM 4 pcs total 4GB

VRAM 4 pcs total 4GB

For designs that have a dedicated ROM device for the GPU video BIOS:

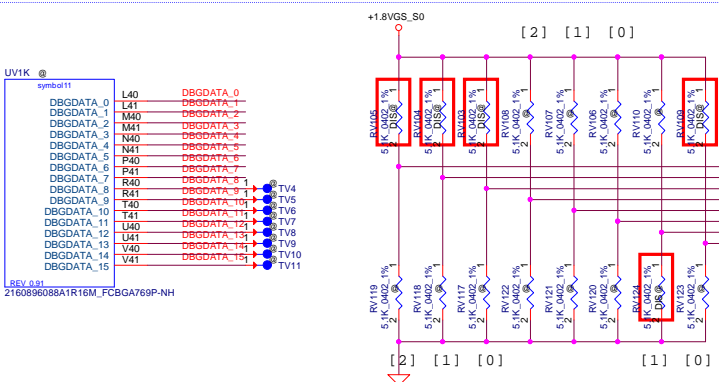
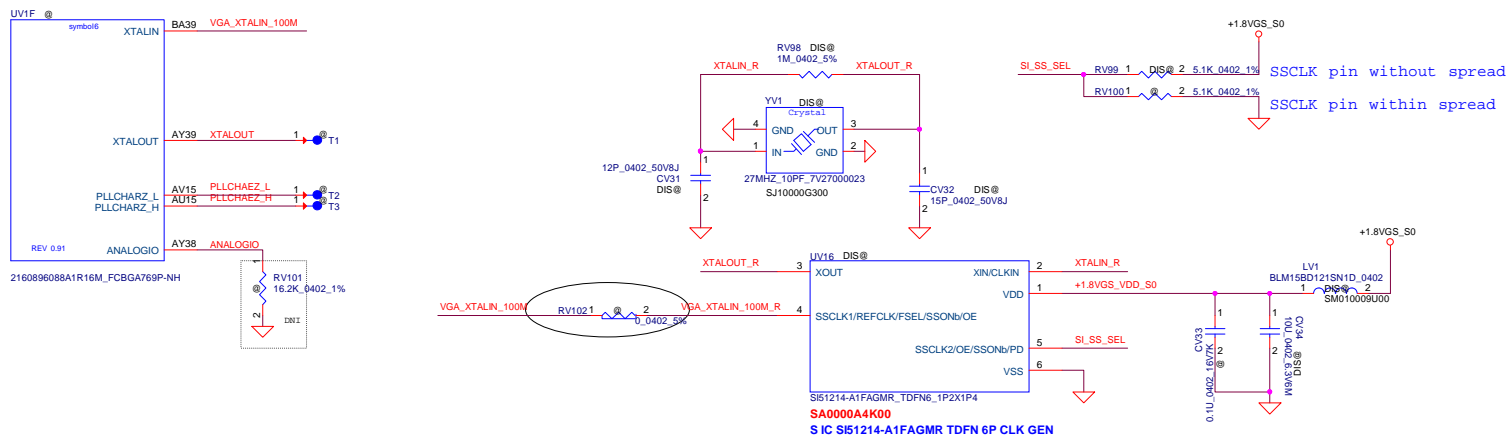
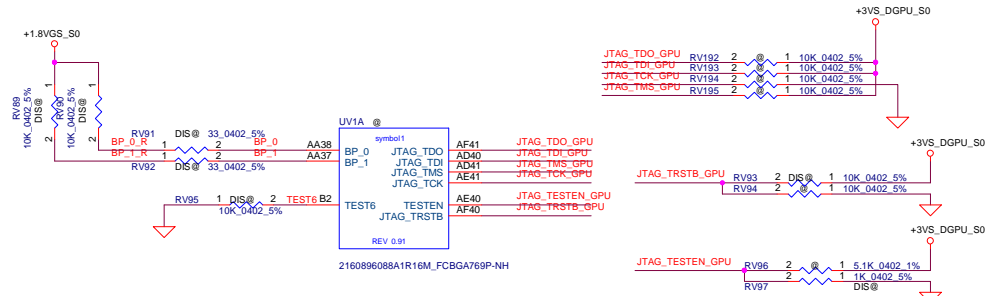
- Use the GPU default strap on GPIO\_22\_ROMCSB (i.e., 1).
- Use the GPU default straps on GPIO\_13, GPIO\_12, and GPIO\_11 (i.e., 101).



BIF_VGA_DIS	GPIO_29	<p>Determine whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space).</p> <p>0: VGA Controller capacity enabled.</p> <p>1: The device will not be recognized as the system's VGA controller (for headless designs).</p>	0 (Internal pull-down)
-------------	---------	---	---------------------------

Size	Document	Number	Rev
Custom		Module Design Topic	0.1





AUD_PORT_CONN[2:0]	
111:	No usable endpoints
110:	One usable endpoint
101:	Two usable endpoints
100:	Three usable endpoints
011:	Four usable endpoints
010:	Five usable endpoints
001:	Six usable endpoints
000:	All endpoints are usable

BOARD_CONFIG[2:0]	
000:	SAM 128Mx32
001:	HYN 128Mx32
010:	MTC 256Mx32
011:	SAM 256Mx32
100:	HYN 256Mx32
101:	MTC 128Mx32
110:	
111:	

DBGDATA[7:6]	
01:	0x 40
00:	0x 41
10:	0x 42
11:	0x 43

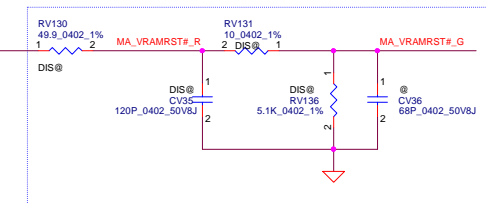
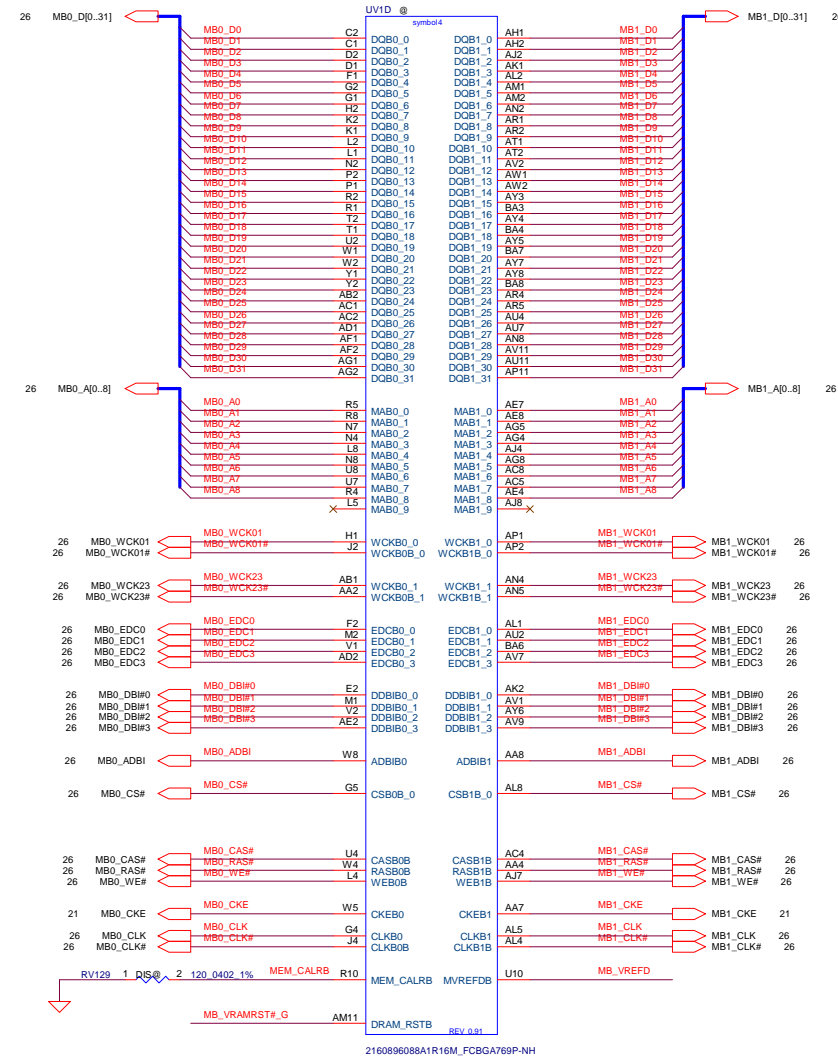
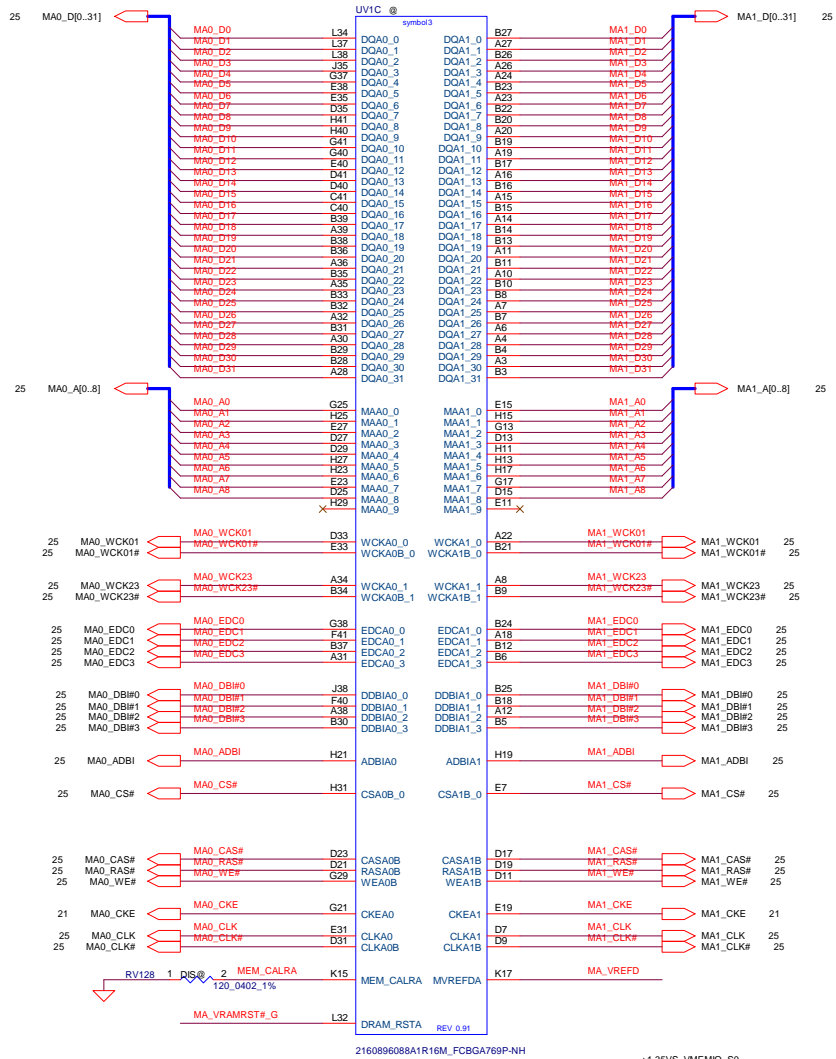
BOARD_CONFIG[2:0]		
2	1	0
RV122 V4G_S@	RV107 V4G_S@	RV106 V4G_S@
S RES 1/16W 5.1K +-1% 0402S SD034510180	S RES 1/16W 5.1K +-1% 0402S SD034510180	S RES 1/16W 5.1K +-1% 0402S SD034510180
RV108 V4G_H@	RV121 V4G_H@	RV120 V4G_H@
S RES 1/16W 5.1K +-1% 0402S SD034510180	S RES 1/16W 5.1K +-1% 0402S SD034510180	S RES 1/16W 5.1K +-1% 0402S SD034510180
RV122 V4G_M@	RV107 V4G_M@	RV120 V4G_M@
S RES 1/16W 5.1K +-1% 0402S SD034510180	S RES 1/16W 5.1K +-1% 0402S SD034510180	S RES 1/16W 5.1K +-1% 0402S SD034510180

Strap Pins		GPU 7-bit Slave Address Field						
DBGDATA_7	DBGDATA_6	A6	A5	A4	A3	A2	A1	A0
LOW	LOW	1	0	0	0	0	0	0
LOW	HIGH	1	0	0	0	0	0	1
HIGH	LOW	1	0	0	0	0	1	0
HIGH	HIGH	1	0	0	0	0	1	1

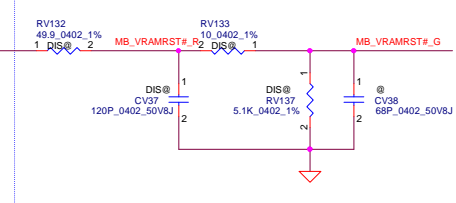
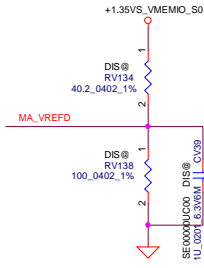
Security Classification		Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2017/07/20	Deciphered Date	2018/07/20		Title	R17M-P1-50/70_(3/9)_MSIC-2
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Size	Document Number
					Custom	Module Design Topic
					Date:	Friday, November 02, 2018
					Sheet	23 of 73

# A0/1 Channel

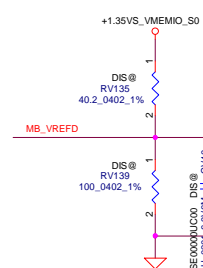
# B0/1 Channel



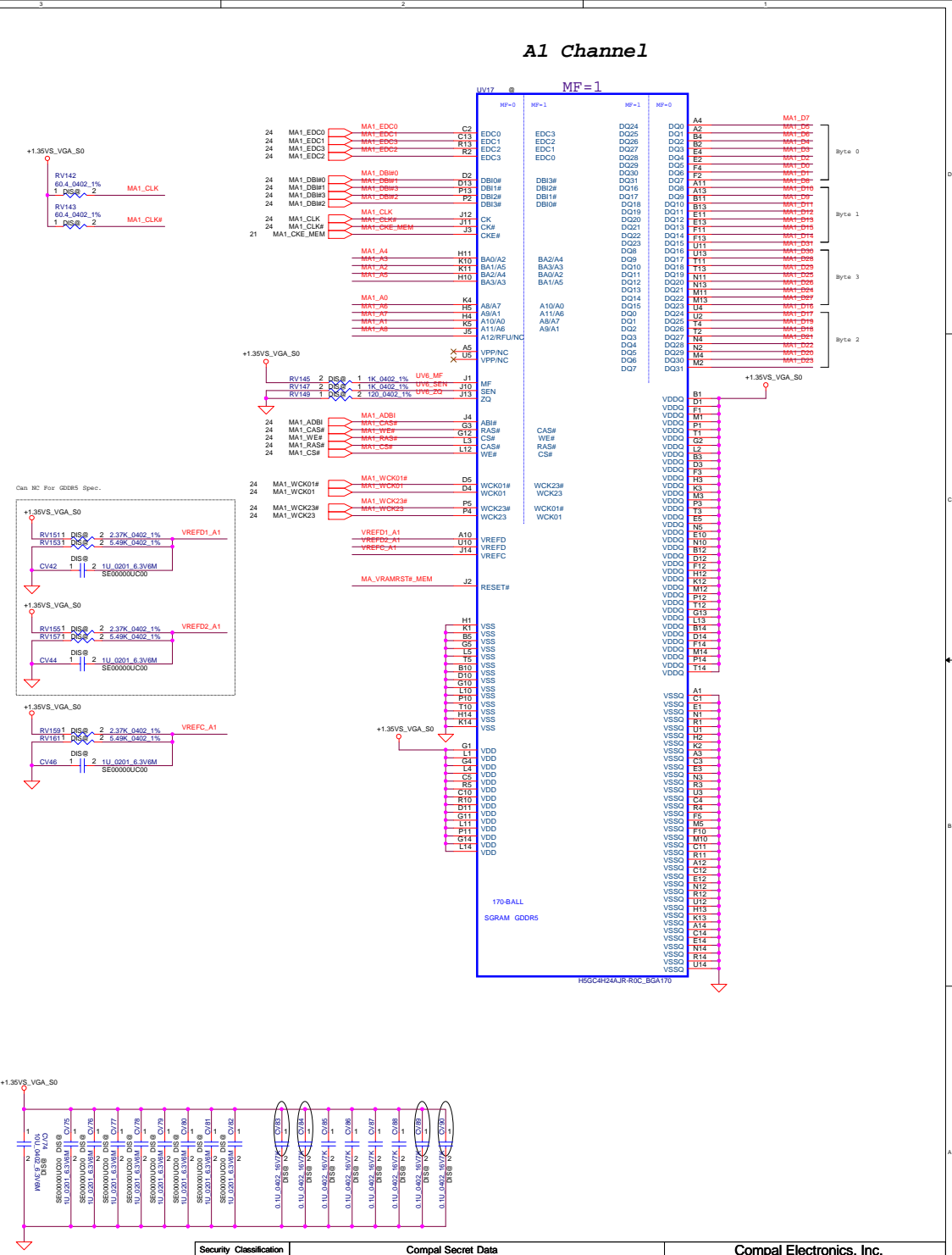
Place close to GPU (within 25mm) and place component within (5mm) close to each other

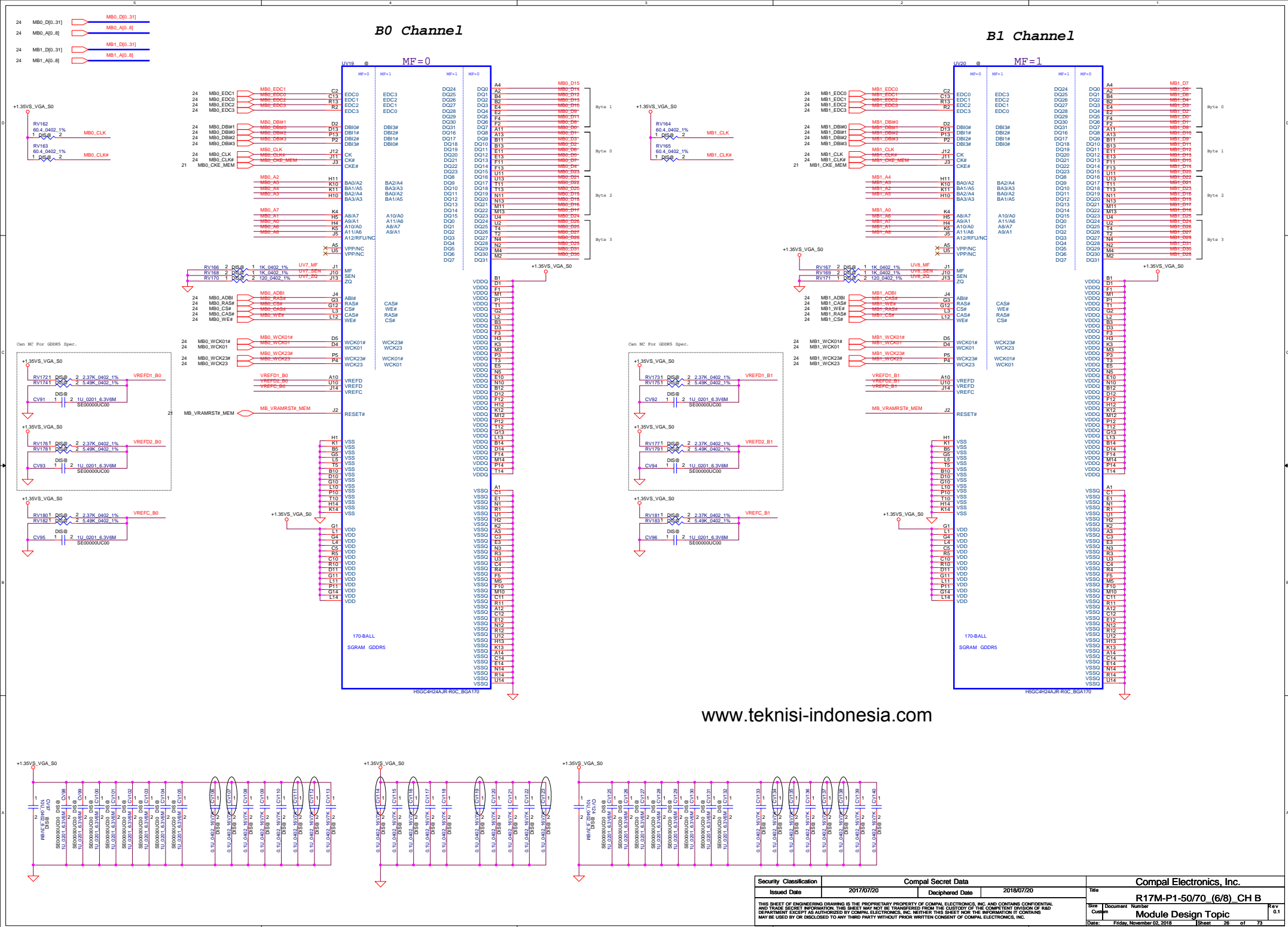


Place close to GPU (within 25mm) and place component within (5mm) close to each other



Security Classification		Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2017/07/20	Deciphered Date	2018/07/20		Title	R17M-P1-50/70_(4/9)_MEM	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Size	Document Number	Rev
					Custom	Module Design Topic	
Date:					Friday, November 02, 2018	Sheet	24 of 73

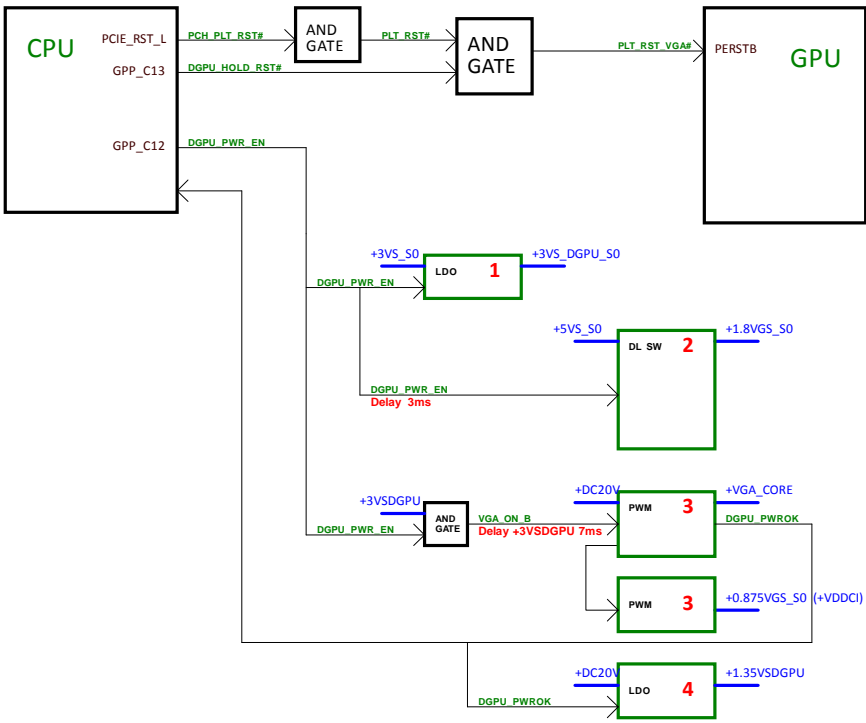
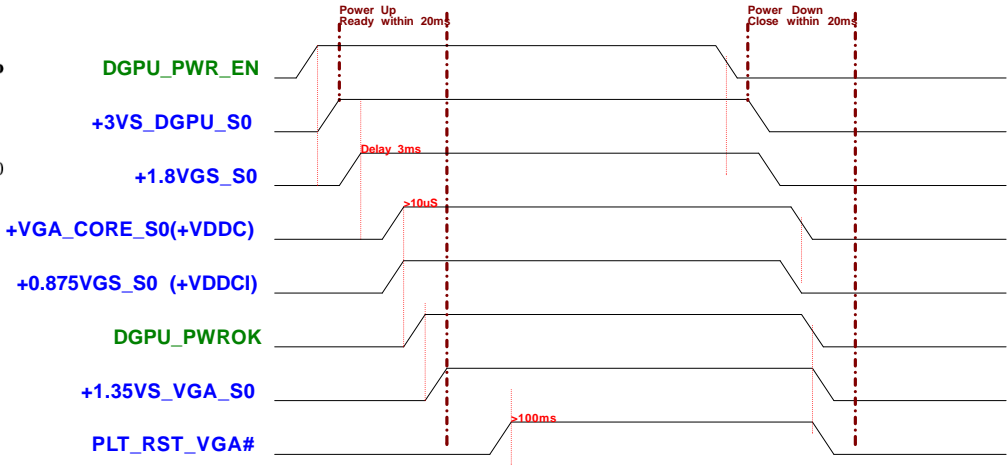
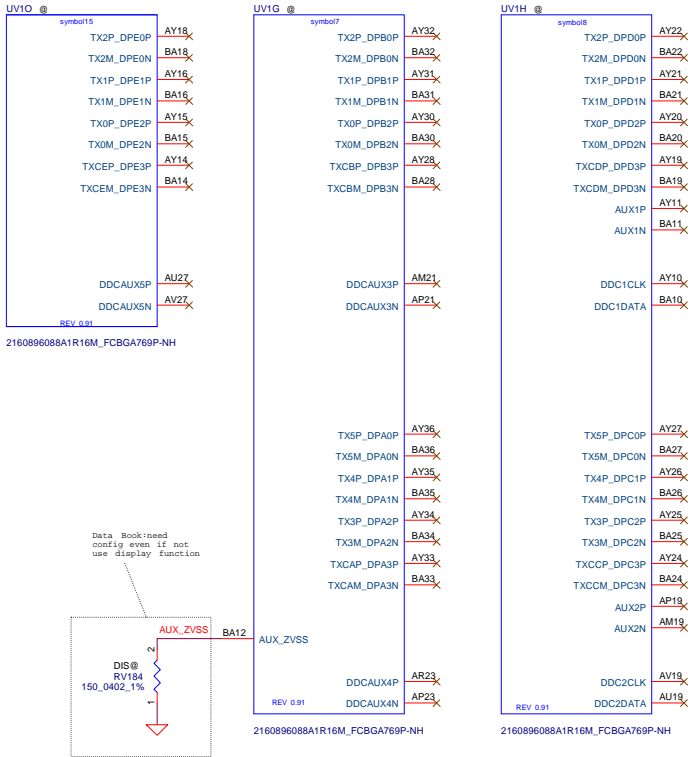




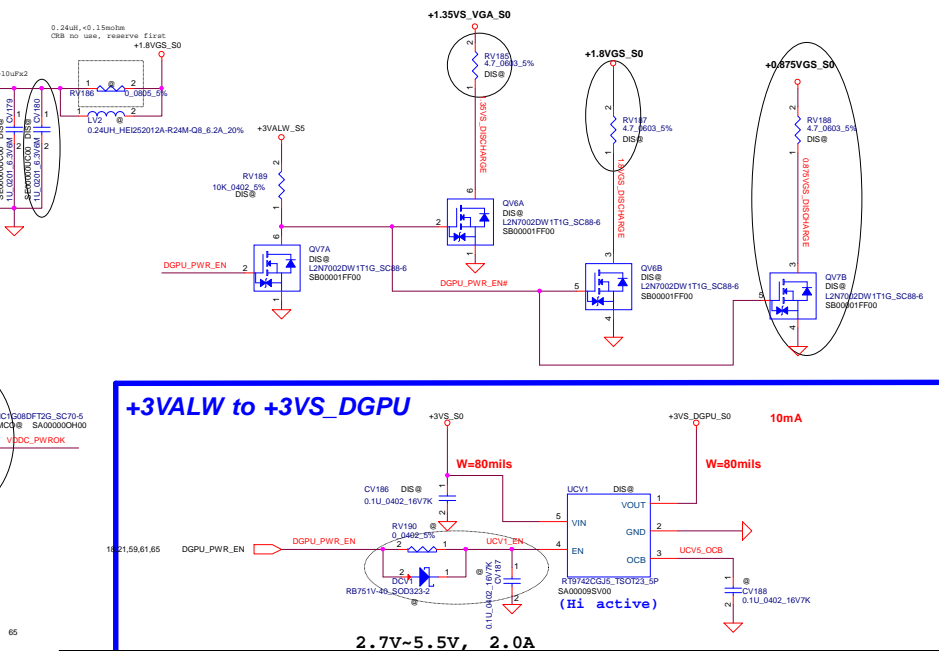
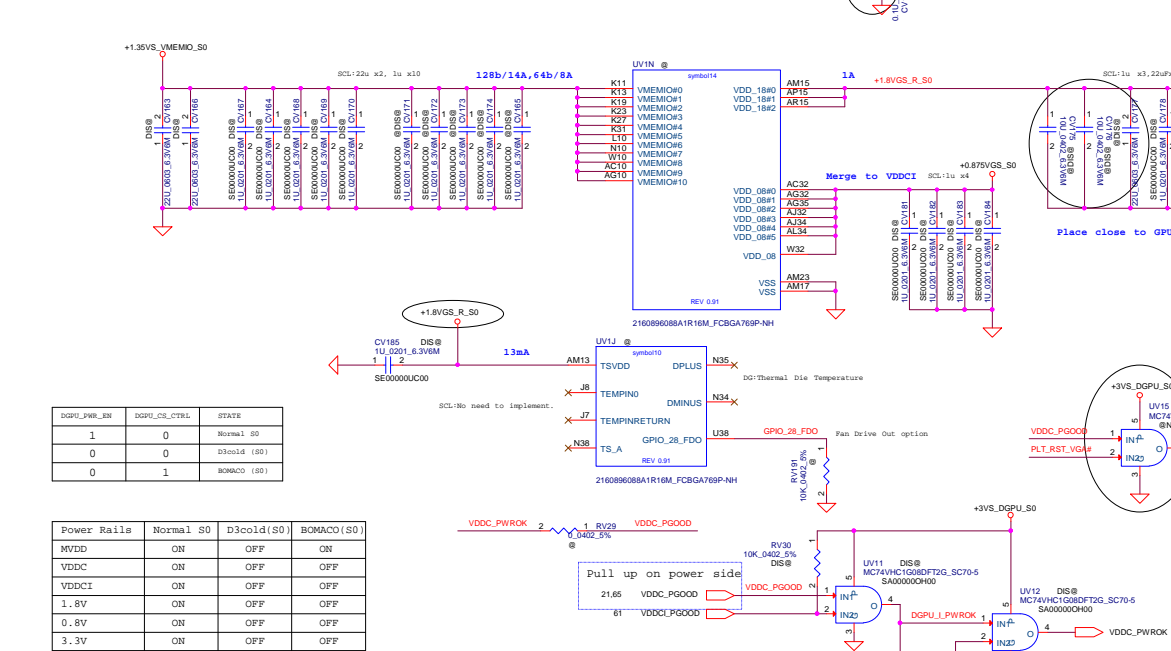
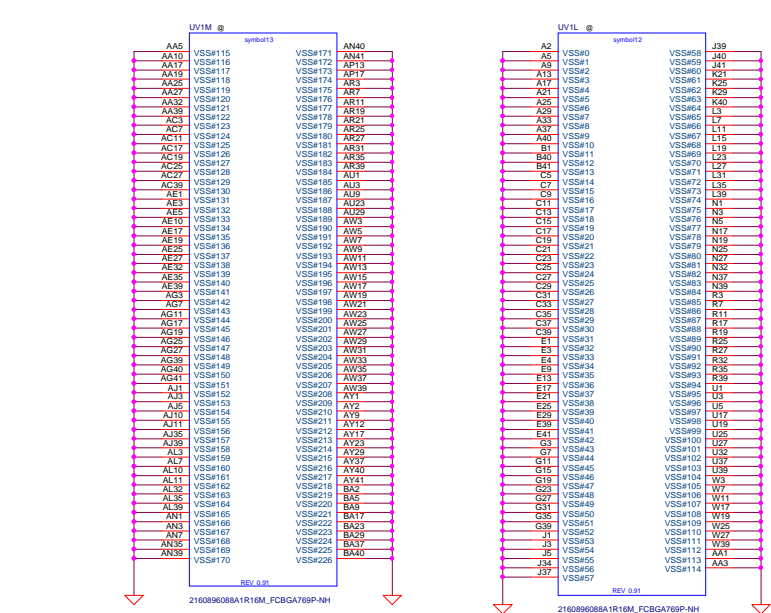
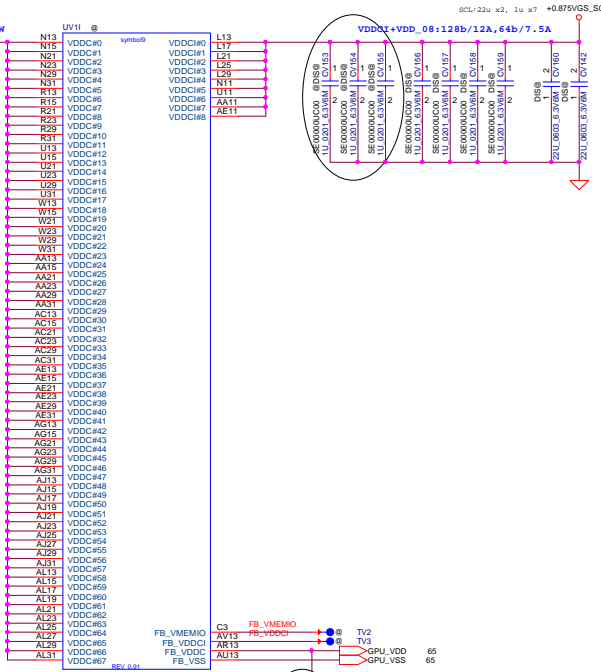
5.3 Power-up/down Sequence

"R17M-P1-50 / R17M-P1-70" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD\_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/μs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 μs before VDDC, VDDCI, VDD\_08, and VMEMIO start to ramp up.



Rail Name		Nominal Voltage	DC Tolerance	AC Tolerance	Maximum Current	Notes
VDDCI	"R17M-M2-70"	0.700 V	± 3%	± 3%	5 A (TDC)	9
VDD_08	"R17M-M2-70"	0.800 V	± 3%	± 3%	1.5 A (TDC)	9
VDDCI	All others	0.875 V	± 3%	± 3%	8 A (TDC)	2
VDD_08						
VMEMIO		1.35 V	± 3%	± 3%	128 bit: 2 A (TDC), 8 A (EDC) 64 bit: 1 A (TDC), 4 A (EDC)	3
VDD_18		1.8 V	± 3%	± 3%	1 A (TDC)	5, 6
VDD_33		3.3 V	± 3%	± 3%	10 mA (TDC)	
TSVDD		1.8 V	± 3%	± 3%	13 mA	7

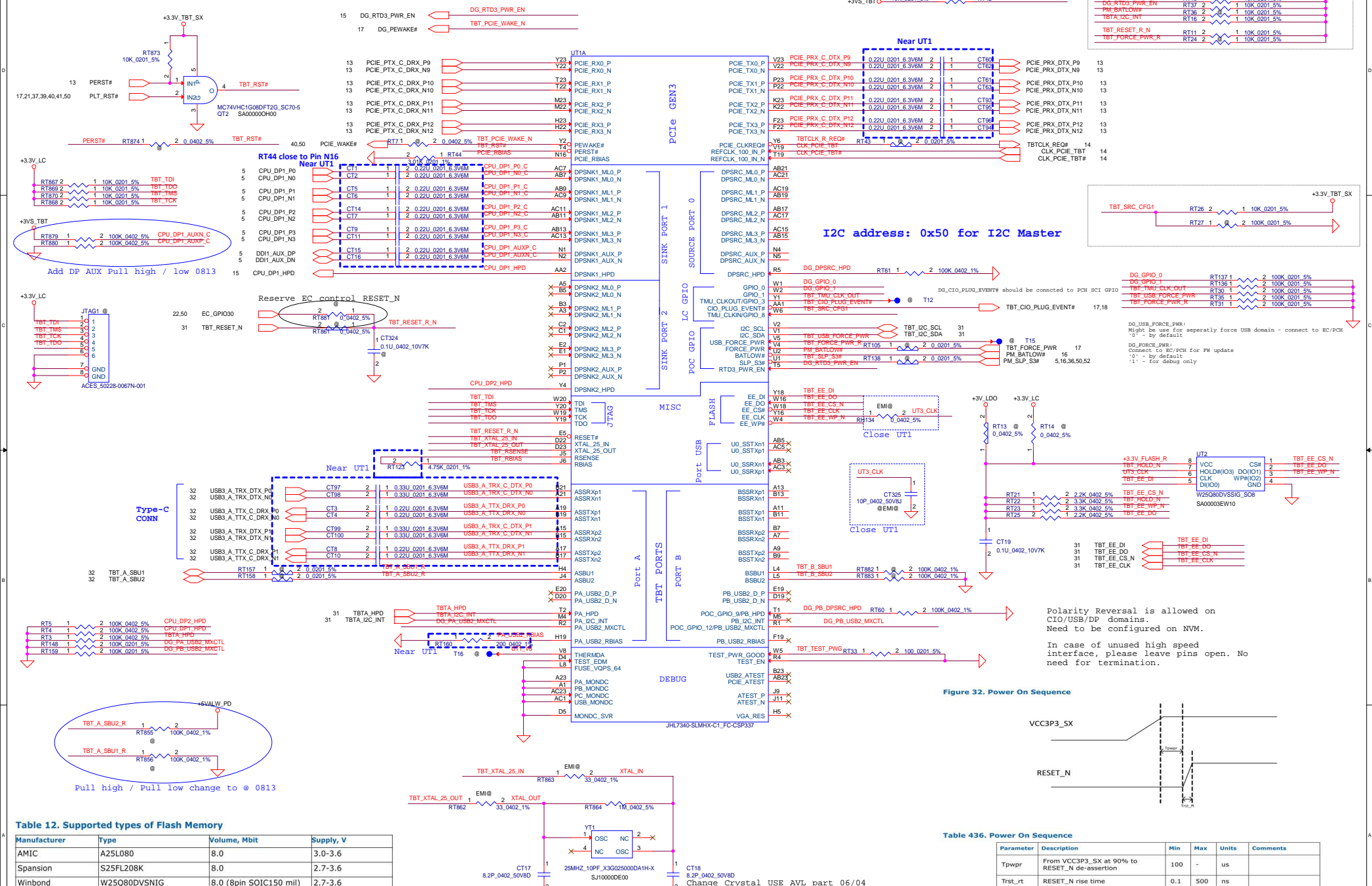


DGPU_PWR_EN	DGPU_CS_CTRL	STATE
1	0	Normal S0
0	0	S3cold (S0)
0	1	S3Wd0 (S0)

Power Rails	Normal S0	D3cold(S0)	BOMACO(S0)
MYDD	ON	OFF	ON
VDDCI	ON	OFF	OFF
1.8V	ON	OFF	OFF
0.8V	ON	OFF	OFF
3.3V	ON	OFF	OFF



## Titan Ridge SP Collateral - TBT, USB & DP Part



<b>Manufacturer</b>	<b>Type</b>	<b>Volume, Mbit</b>	<b>Supply, V</b>
AMIC	A25L080	8.0	3.0-3.6
Spanion	S25FL208K	8.0	2.7-3.6
Winbond	W25Q80DVSNIG	8.0 (8pin SOIC150 mil)	2.7-3.6
Macronix	MX25L8006EM1I	8.0 (150mil, 8-SOP)	2.7-3.6
Micron	M25PE80-VMN6TP	8.0 (150mil, SO8N)	2.7-3.6
Micron	M25PX80-VMN6TP	8.0 (150mil, SO8N)	2.3-3.6

### Table 436. Power On Sequence

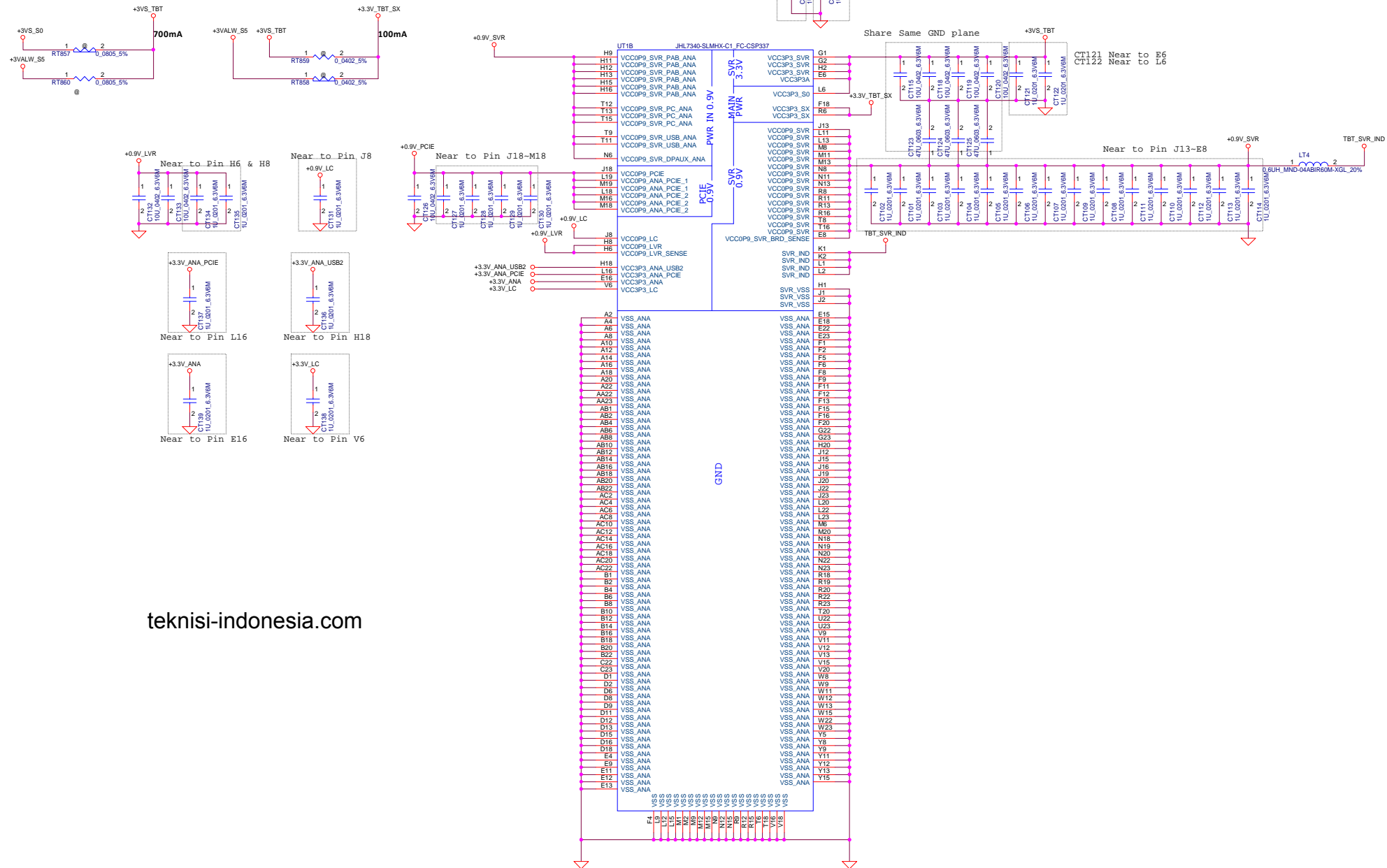
Parameter	Description	Min	Max	Units	Comments
Tpwpr	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us	
Trst_rt	RESET_N rise time	0.1	500	ns	

Security Classification	Compal Secret Data		
Issued Date	2016/06.23	Deciphered Date	2017/06/23
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>			

<b>Compal Electronics, Inc.</b>			
Title <b>Thunderbolt TR(1/4)</b>			
Size	Document Number	Rev	
	<b>LA-G801P</b>	<b>0.1</b>	
Date:	Friday, November 02, 2018	Sheet	29 of 73



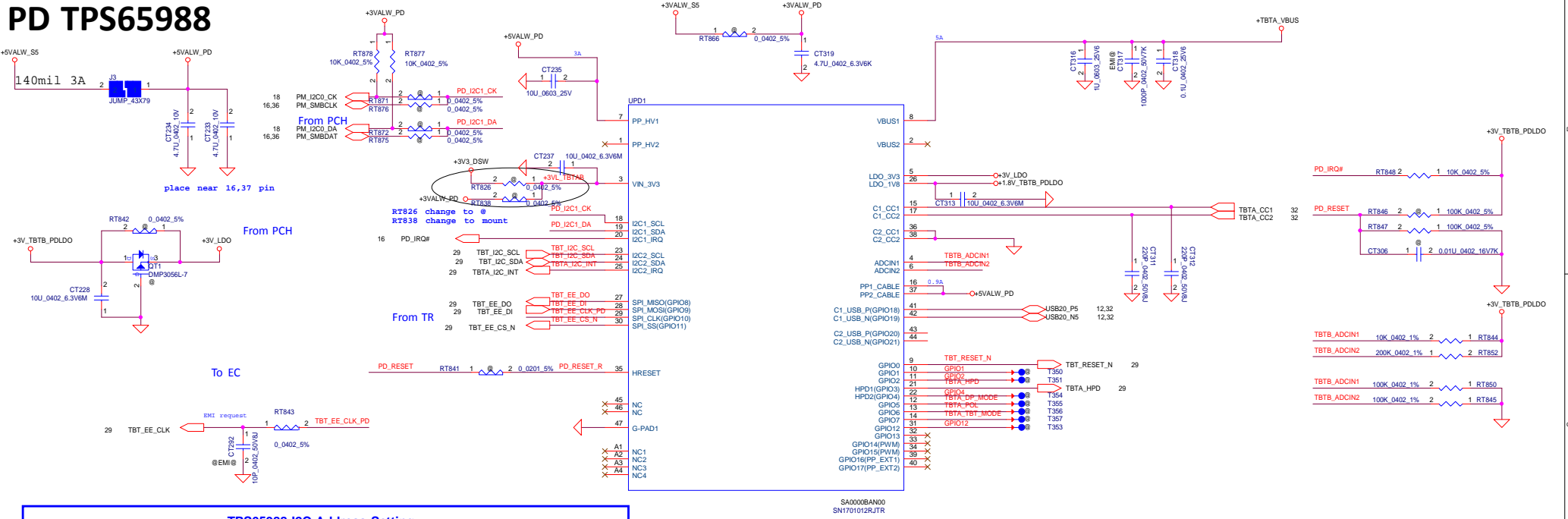
## Titan Ridge SP Collateral - Power/GND



teknisi-indonesia.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2016/06/23	Deciphered Date		2017/06/23	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THRID PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title		
				Thunderbolt TR(2/4)		
				Size	Document Number	Rev
				LA-G801P		0.1
Date:		Friday, November 02, 2016		Sheet	30	of 73

**PD TPS65988**



## TPS65988 I2C Address Setting

### Table 8. I<sup>2</sup>C Address Selection

DIV = R2/(R1+R2) <sup>(1)</sup>		I <sup>2</sup> C UNIQUE ADDRESS [3:1]	
DIV_min	DIV_max	I2C_ADDR_DECODE_C1	I2C_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

**Table 4. I<sup>2</sup>C Default Unique Address I2C1 - Port 1**

Default I <sup>2</sup> C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE_C1[2:0]			R/W

Note 1: Any bit is maskable for each port independently providing firmware override of the I<sup>2</sup>C address.

Note 1: Any bit is maskable for each port independently providing firmware override of the I<sup>2</sup>C address

Table 5. I<sup>2</sup>C Default Unique Address I2C1 - Port 2

Default <i>PC</i> Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE_C2[2:0]			R/W

Note 1: Any bit is maskable for each port independently providing firmware override of the *PC* address.

Note 1: Any bit is maskable for each port independently providing firmware override of the I<sup>2</sup>C address

For the I2C2 interface, the unique I<sup>2</sup>C address is a fixed value as shown in Table 6 and Table 7.

Table 6. I<sup>2</sup>C Default Unique Address I2C2 - Port 1

Default PC Unique Address								
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	1	1	1	0	0			R/W

Note 1: Any bit is maskable for each port independently, providing firmware override of the PC address.

Note 1: Any bit is maskable for each port independently, providing firmware override of the I<sup>2</sup>C address.

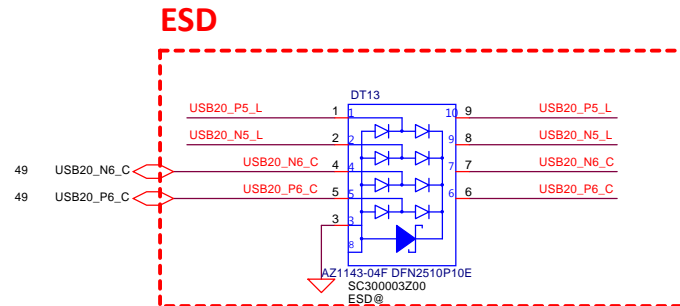
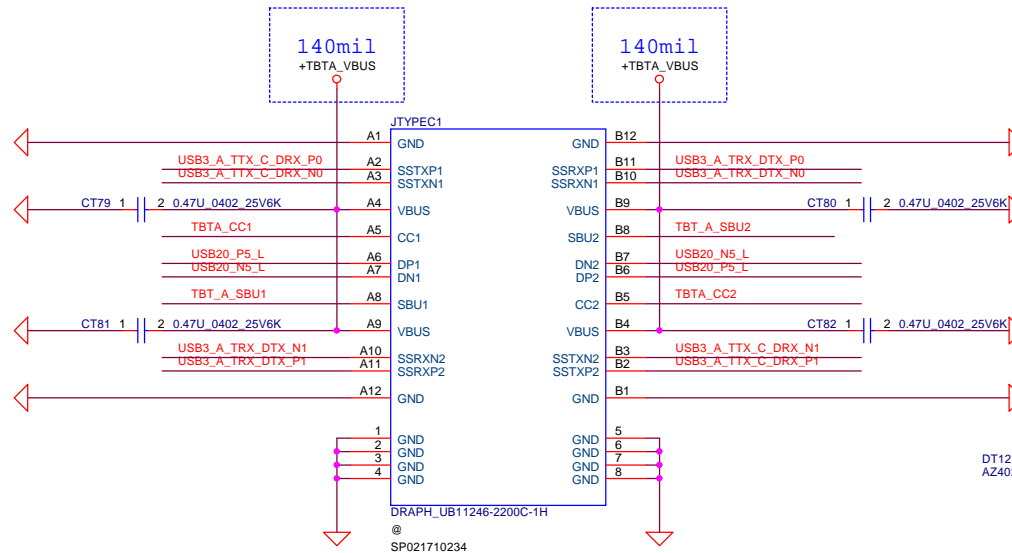
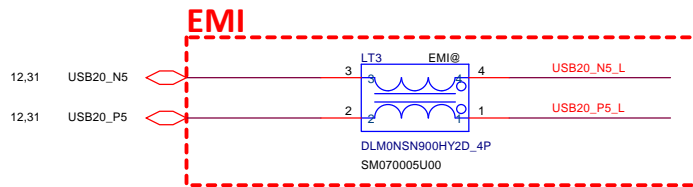
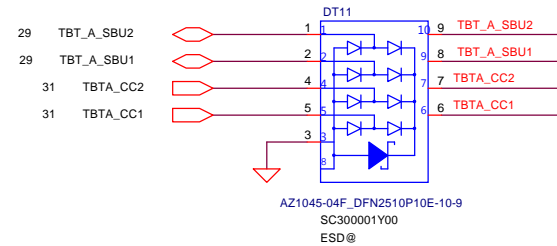
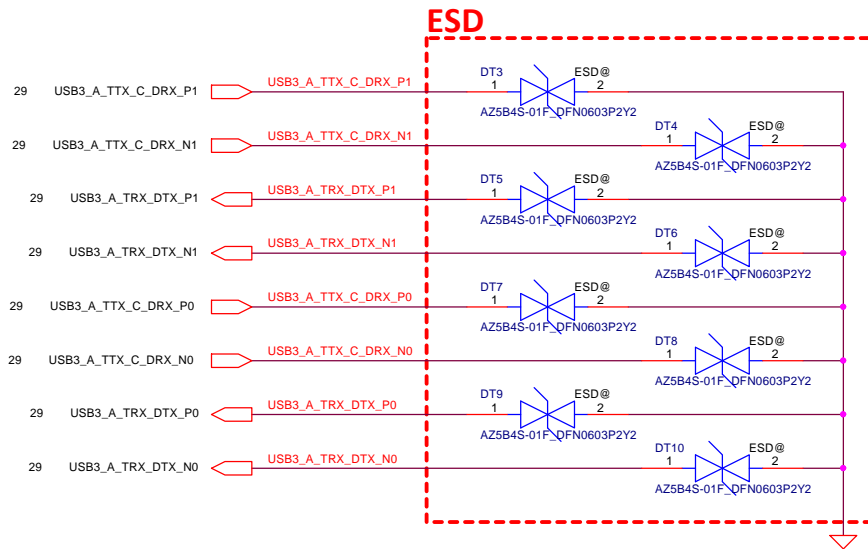
### Table 7. I<sup>2</sup>C Default Unique Address I2C2 - Port 2

Default PC Unique Address								
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	1	1	1	1	1	1	1	R/W

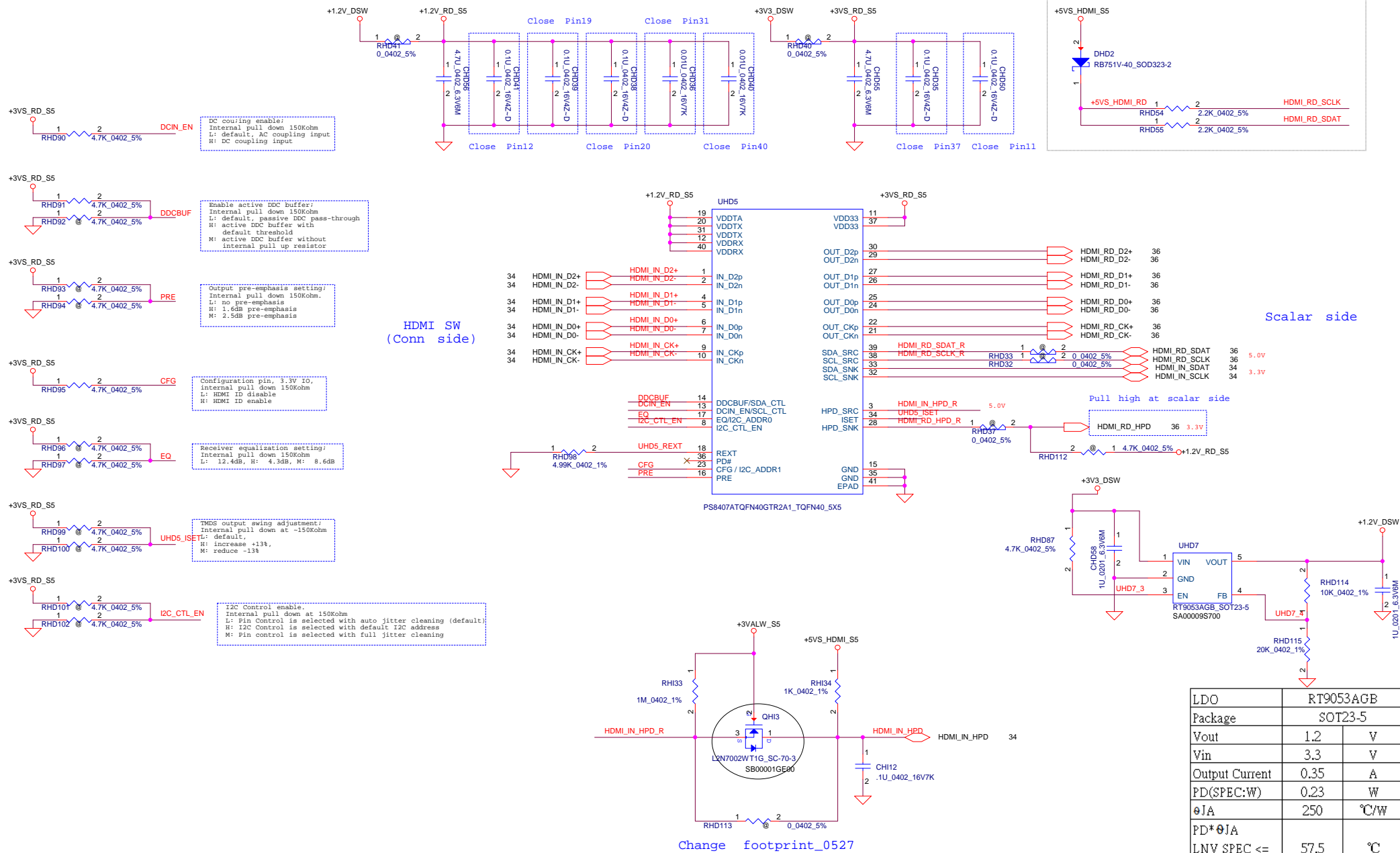
Note 1: Any bit is maskable for each port independently, providing firmware override of the PC address.

Note 1: Any bit is maskable for each port independently, providing firmware override of the I<sup>2</sup>C address.

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>										
Issued Date		2016/06/23		Deciphered Date		2017/06/23		Title	<b>Thunderbolt PD(3/4)</b>					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								Size	Document Number	Rev				
											<b>LA-G801P</b>			1.0
								Date:	Friday, November 02, 2018			Sheet	31	of



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2016/06.23	Deciphered Date		2017/06/23	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						USB3.1 TypeC
Size	Document Number					Rev
LA-E581P						
Date:	Friday, November 02, 2018				Sheet 32 of 73	

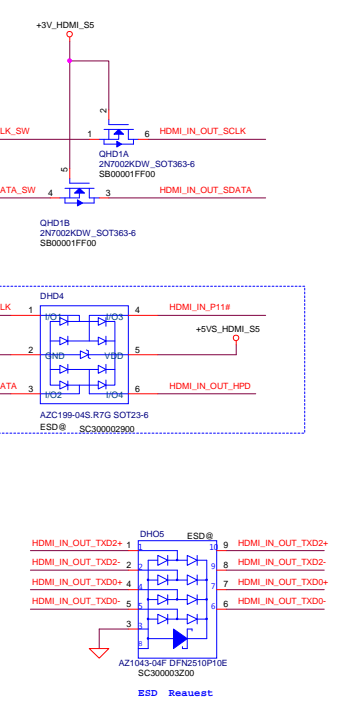
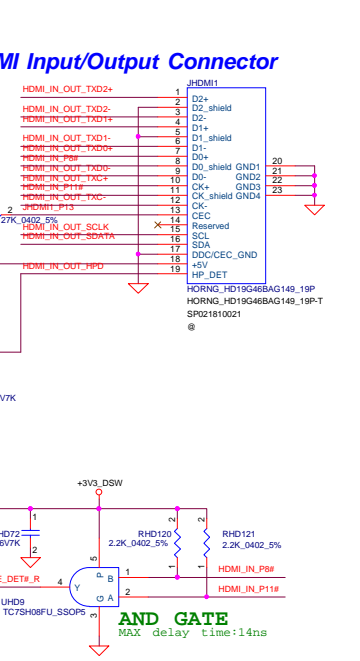
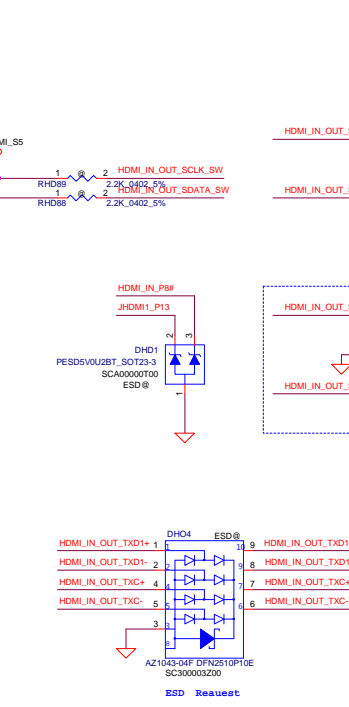
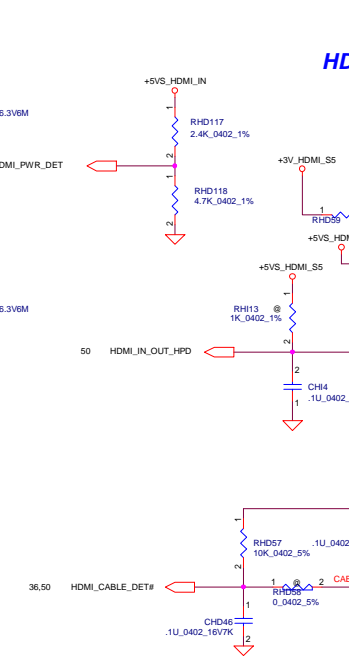
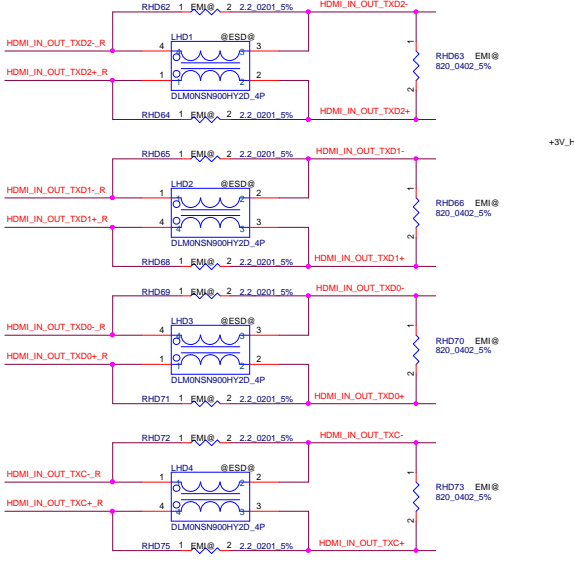
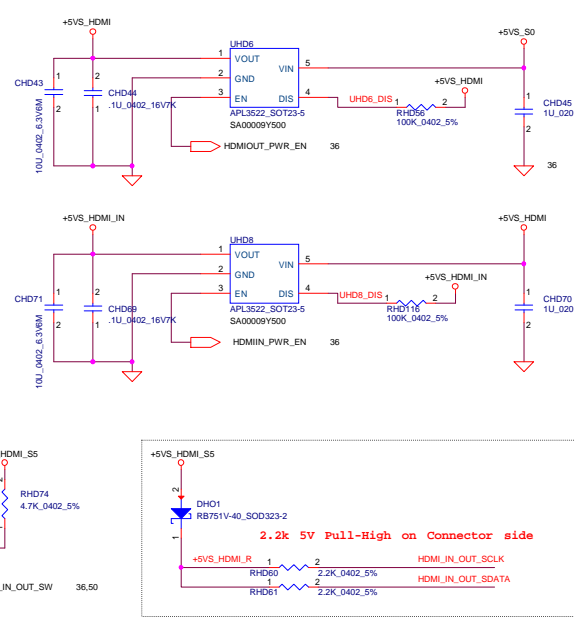
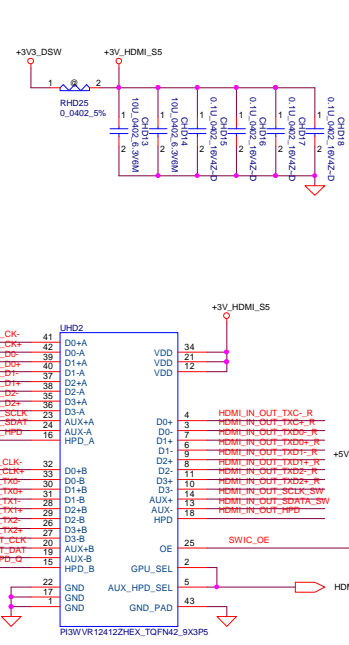
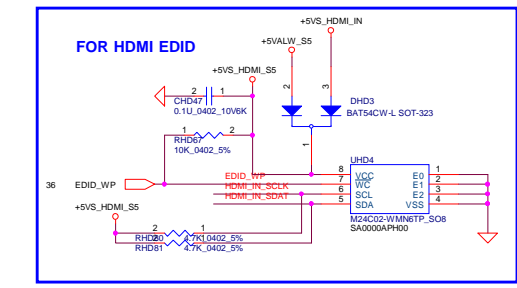
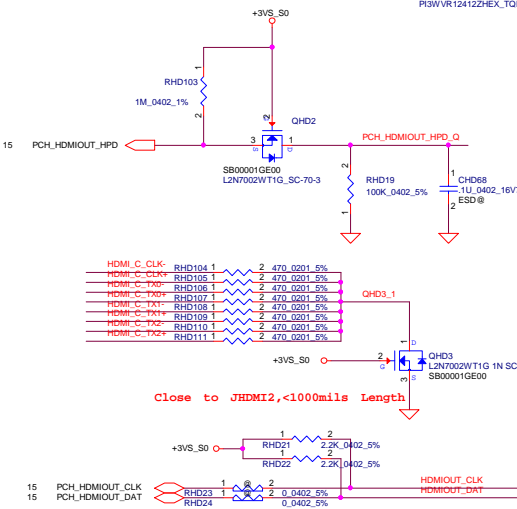


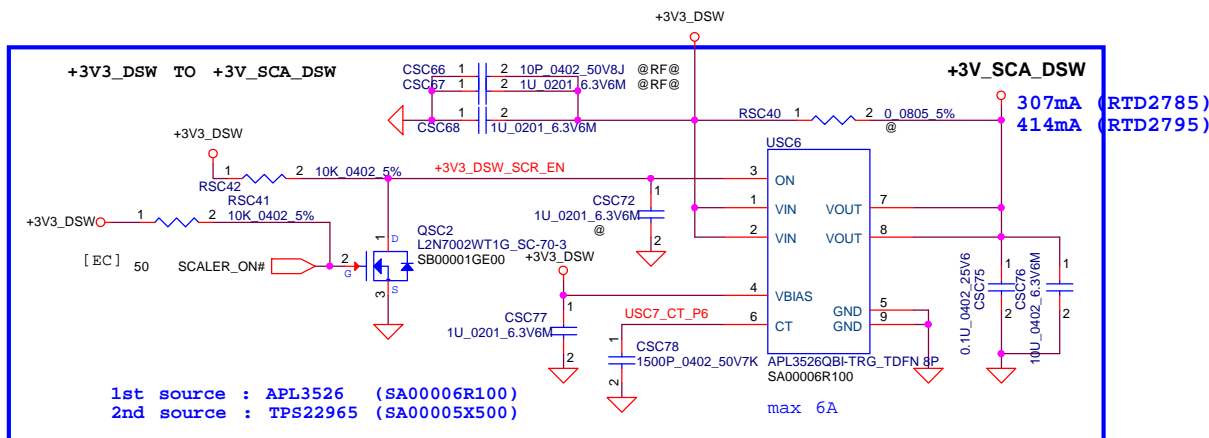
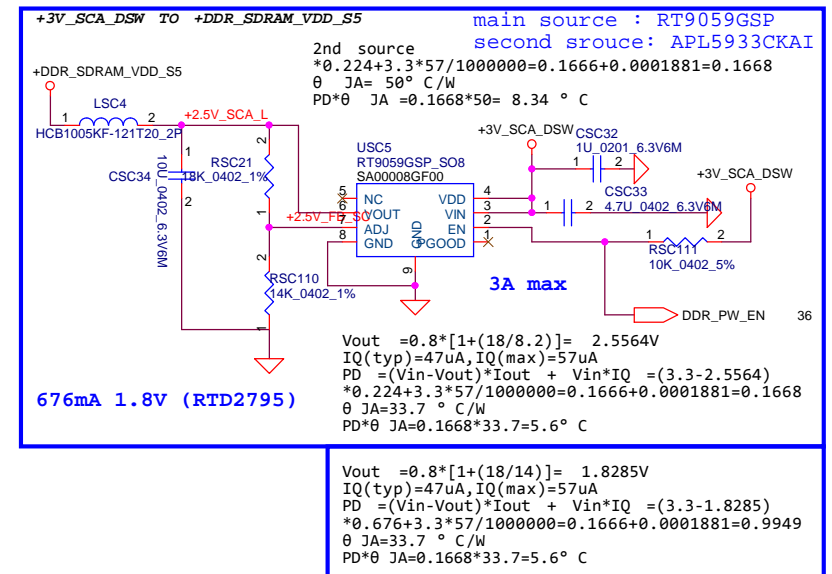
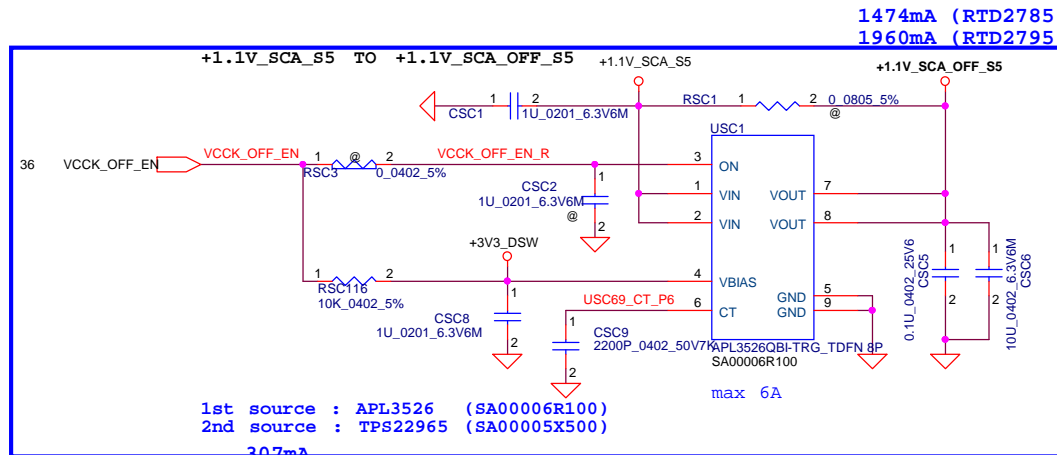
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2015/12/25		Deciphered Date		2015/10/02		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						HDMI OUT LEVEL shift					
						Size		Document Number		Rev	
						LA-F881P M/B					
						Date:		Friday, November 02, 2018		Sheet 33 of 73	

Control			Switch Function		
OE	GPU_SEL	AUX_HPD_SEL	D0-D3	AUX	HPD
High	Low	Low	A	AUX A	HPD A
High	Low	High	A	AUX B	HPD B
High	High	Low	B	AUX A	HPD A
High	High	High	B	AUX B	HPD B
Low	X	X	Hi-Z	Hi-Z	Hi-Z

RTD2785  
RTD2795

CPU HDMI-OUT

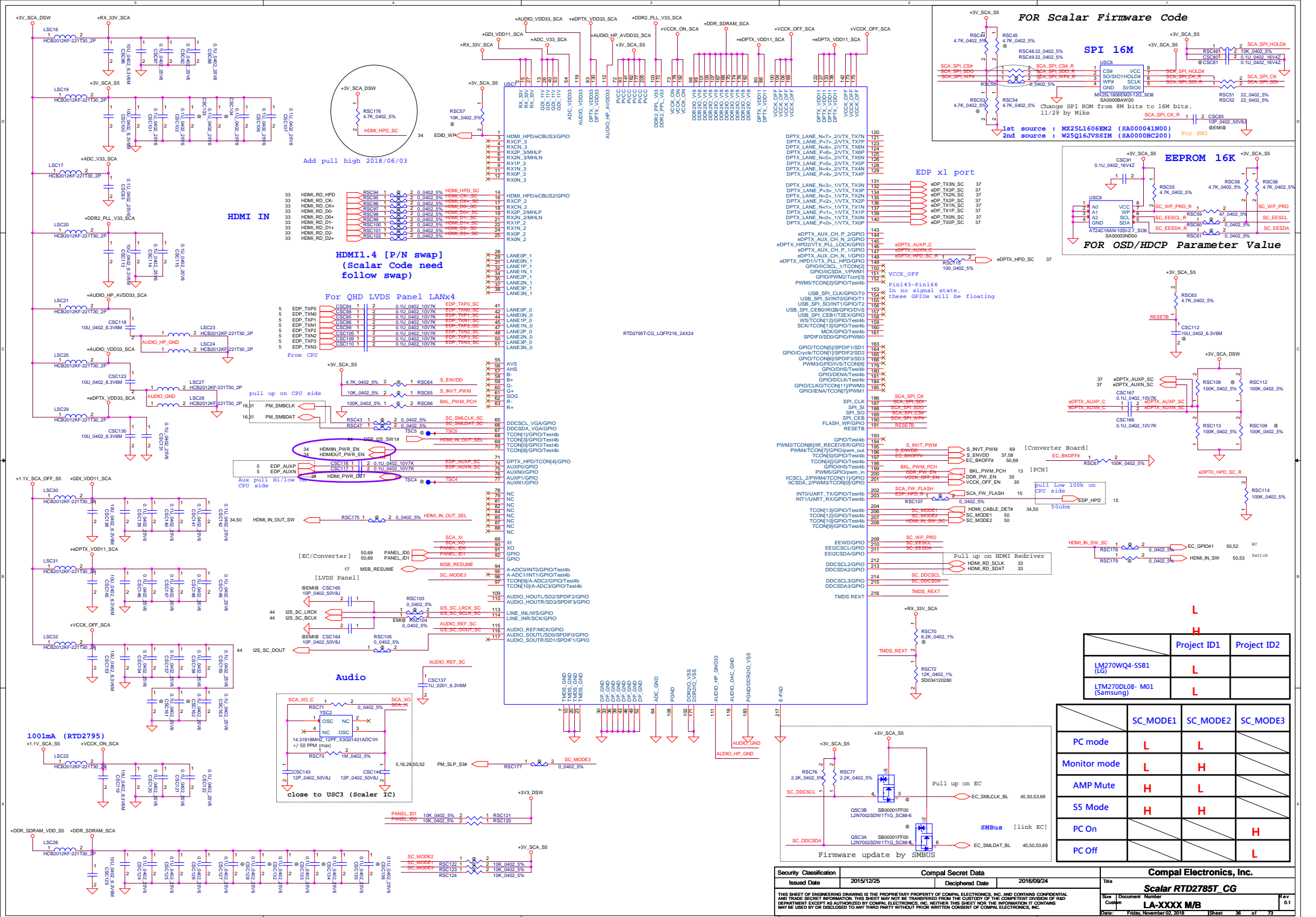




www.teknisi-indonesia.com

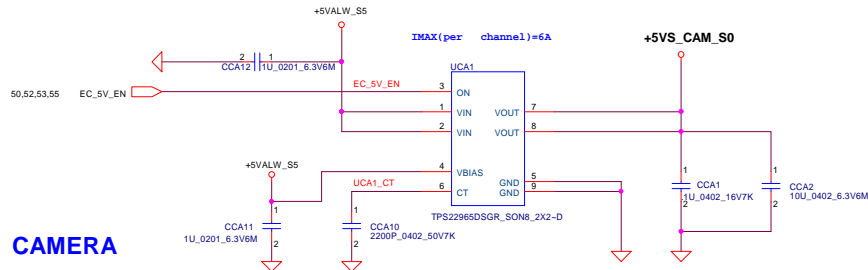
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Scalar Power	
				Size B	Document Number
				LA-XXXX M/B	
Date: Friday, November 02, 2018				Sheet	35 of 73
				Rev	0.1





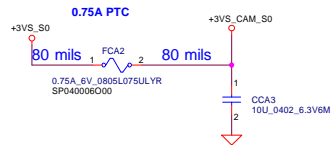


## +5VALW\_S5 to +5VS\_CAM\_S0 Transfer



CAMERA

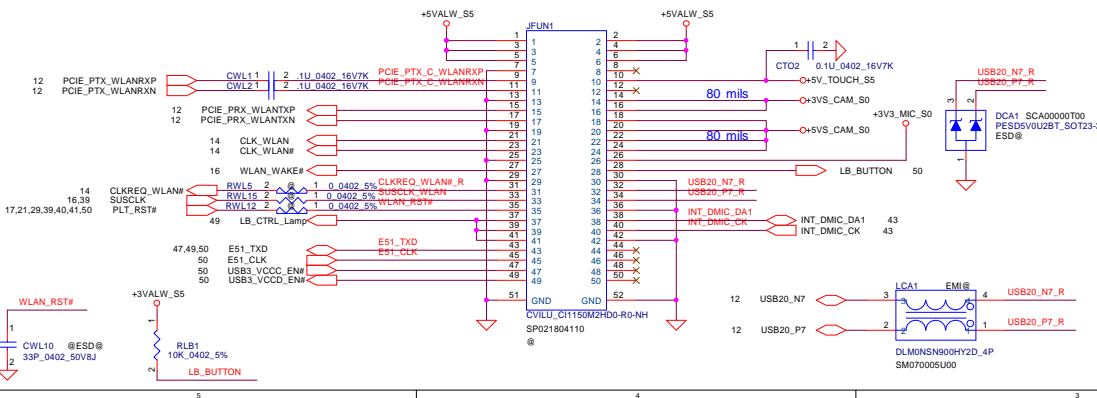
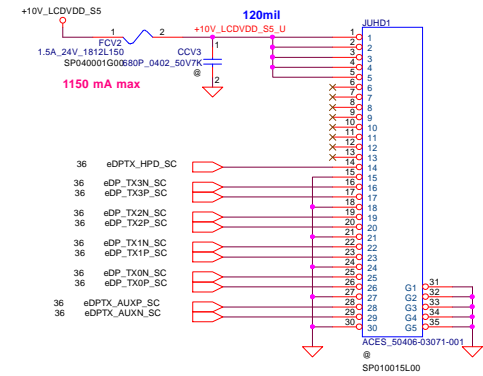
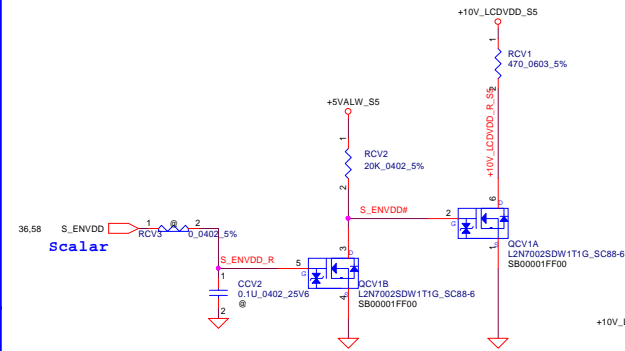
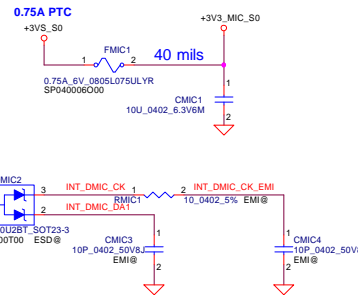
1st source : APL3526 (SA00006R100)  
2nd source : TPS22965 (SA00005X50L)



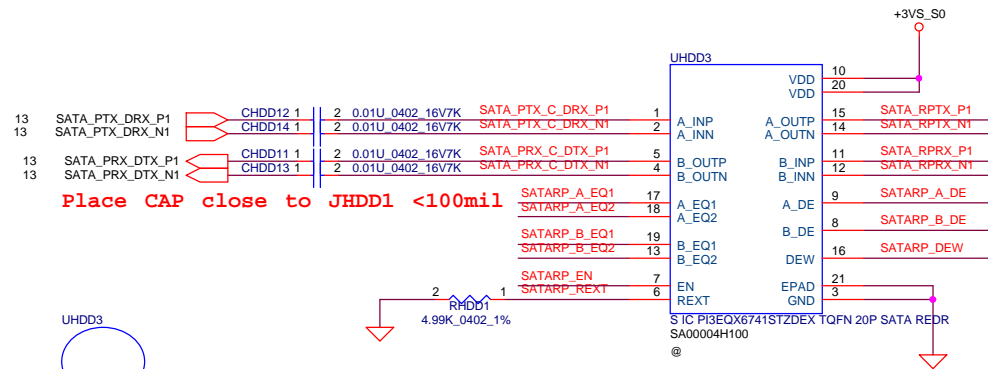
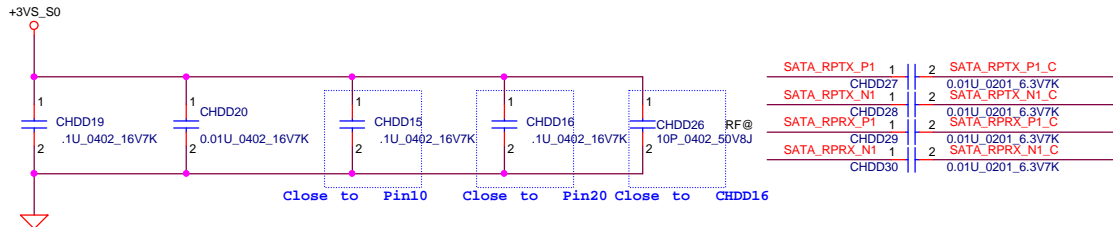
Touch



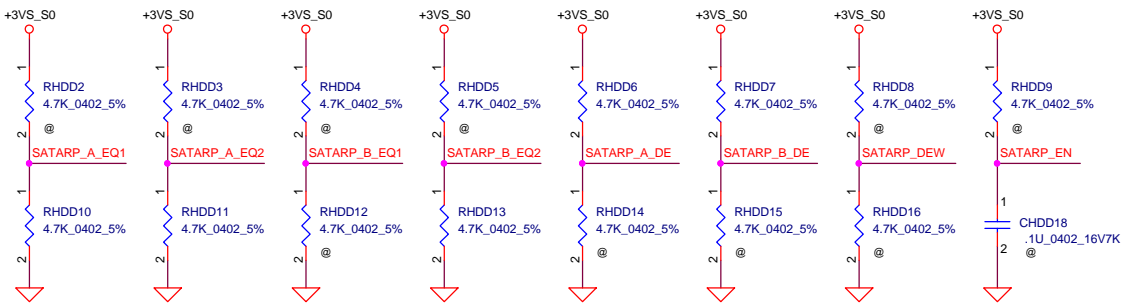
MIC



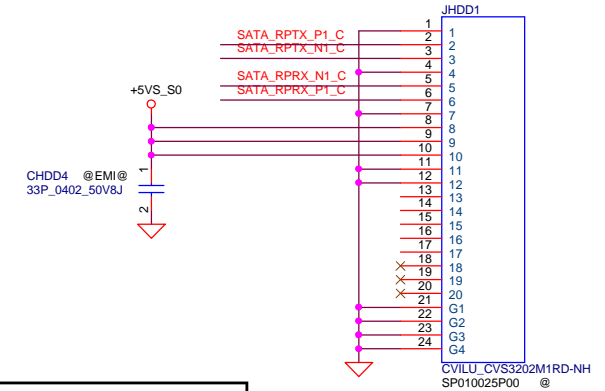
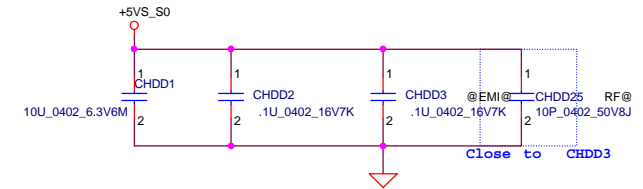
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				LA-E631P M/B
Date: Friday, November 02, 2018				Rev 0.1



PS8527CTQFN20GTR2A2\_TQFN20\_4X4  
SA00007JU10

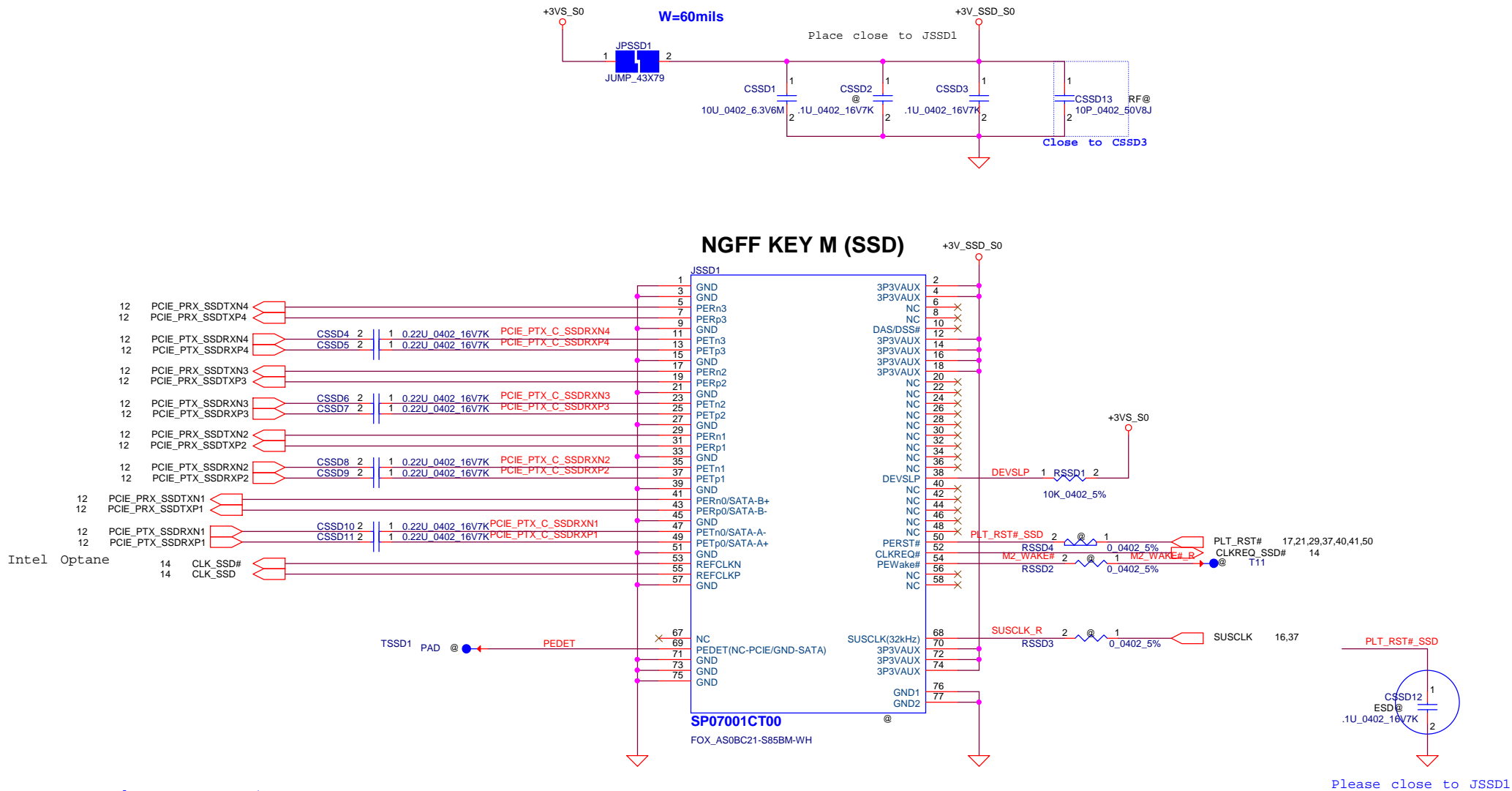


## SATA HDD Conn.



A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				HDD/ODD	
Size	Document	Number	Rev	LA-F881P M/B	
Custom			0.1		
Date:	Friday, November 02, 2018	Sheet	38 of 73		



GPIO Control BIOS SEL PCIe/SATA

Module Configuration Decodes				Module Type and Main Host Interface <sup>1</sup>	Port Configuration <sup>2</sup>
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				SSD (M2)	
				Size B	Rev 0.1
				LA-F881P M/B	
				Date:	Friday, November 02, 2018
				Sheet	39 of 73

**WOL circuit (Connect +3V\_LAN to +3VALW)**

Diagram illustrating the WOL circuit (Connect +3V\_LAN to +3VALW). The circuit shows a connection between +3VALW\_S5 and +3.3V\_LAN\_S5, with a 60mil trace length on each side. The central component is labeled JUM1 @ JUMP 43X39, with pins 1 and 2. The current is specified as 300mA, 120ohm.

**+3.3V\_LAN rising time (10%~90%) need > 0.5ms and <100ms.**

\_\_\_\_\_

**Power (Decoupling Cap.)**

**40 mils**

+3.3V\_LAN\_SS **Close to Pin 11,23**

CL1 1 2 .1U .0402 16V7K

CL2 1 2 .1U .0402 16V7K

@ CL5 1 2 4.7U .0402 6.3V6M

@ CL21 1 2 4.7U .0402 6.3V6M

@ CL8 1 2 4.7U .0402 6.3V6M

CL3 1 2 .1U .0402 16V7K

**Close to Pin 32**

**60 mils**

+LAN\_VDDREG

CL4 1 2 .1U .0402 16V7K

CL6 1 2 .1U .0402 16V7K

CL7 1 2 .1U .0402 16V7K

CL9 1 2 .1U .0402 16V7K

**Close to pin 3,8,30,24**

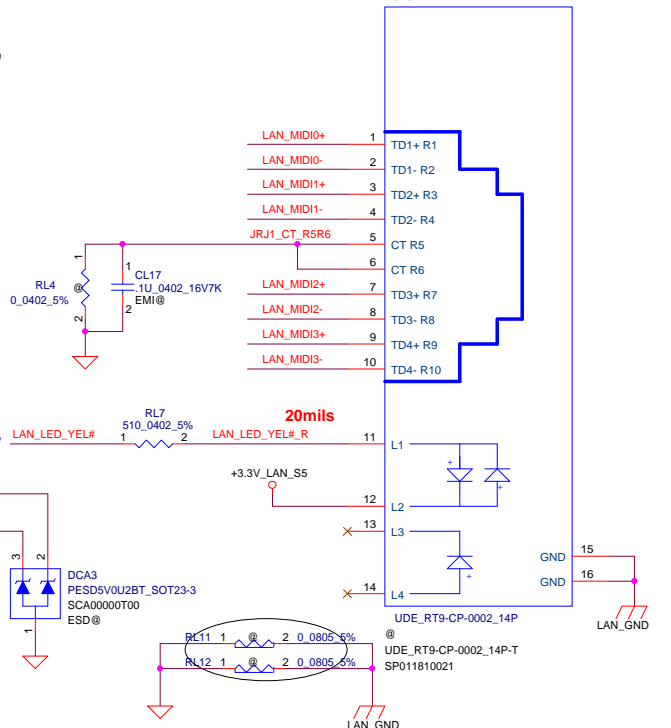
WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

always on

blinking

Diagram illustrating the layout of the RTL8111G-CG\_0ohm resistor. The layout shows a 3x3 grid of resistors. The labels for the resistors are as follows:

- Top Row: RL14 LANG@ SD028000080, RL17 LANG@ SD028000080, RL20 LANG@ SD028000080
- Middle Row: RL15 LANG@ SD028000080, RL18 LANG@ SD028000080, RL21 LANG@ SD028000080
- Bottom Row: RL16 LANG@ SD028000080, RL19 LANG@ SD028000080, JRJ1

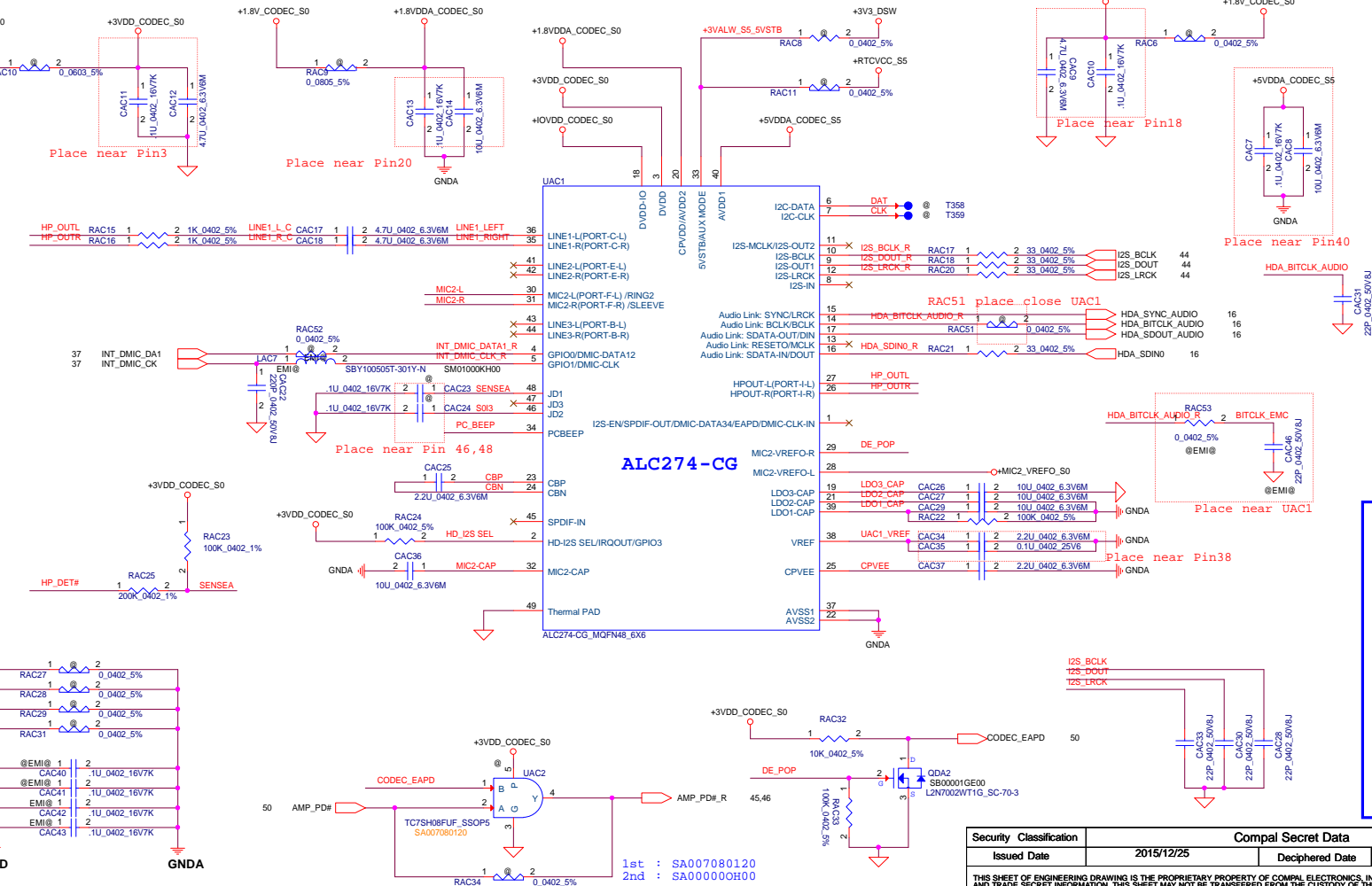
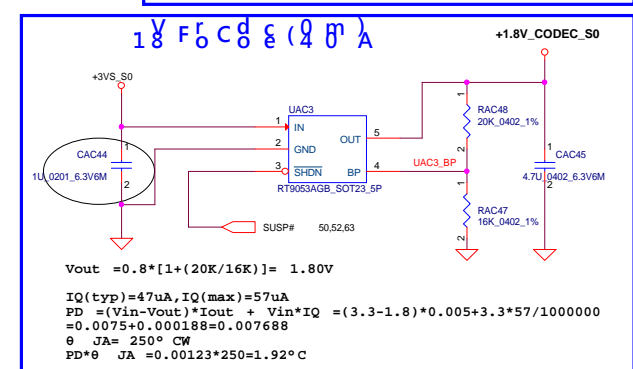
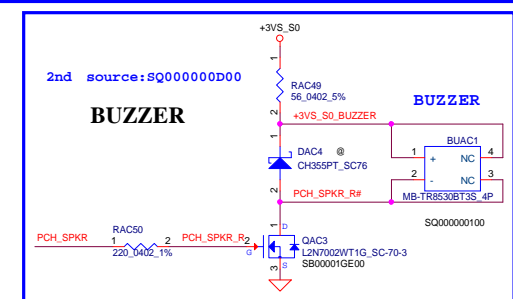
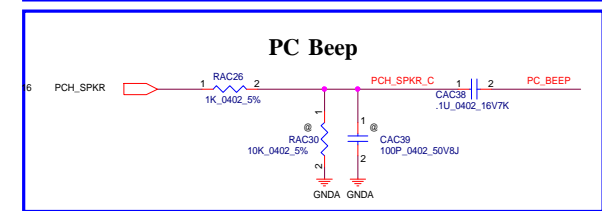
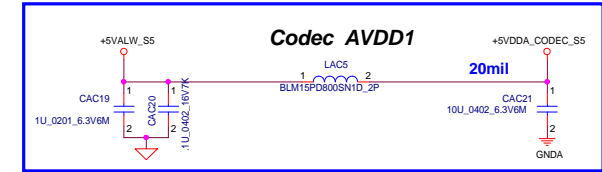
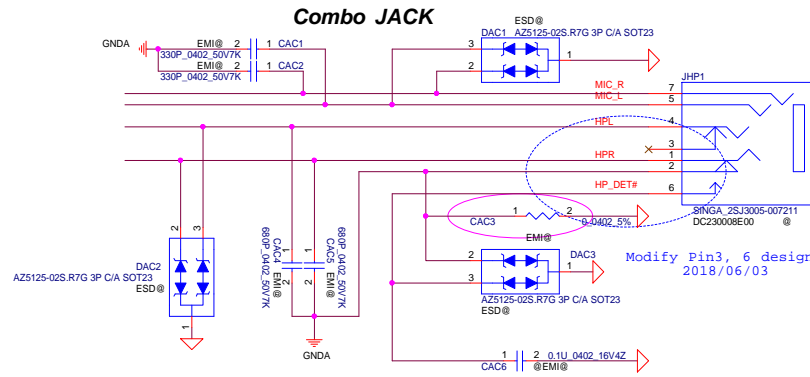
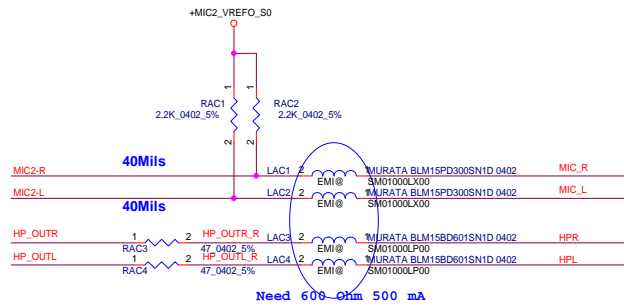


Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>LAN RTL8111G/H</b>	
Issued Date	2015/12/25	Deciphered Date	2016/12/15	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Document	Number
				LA-E881P W/B Date: Friday, November 02, 2018 Sheet 40 of 73	

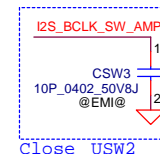
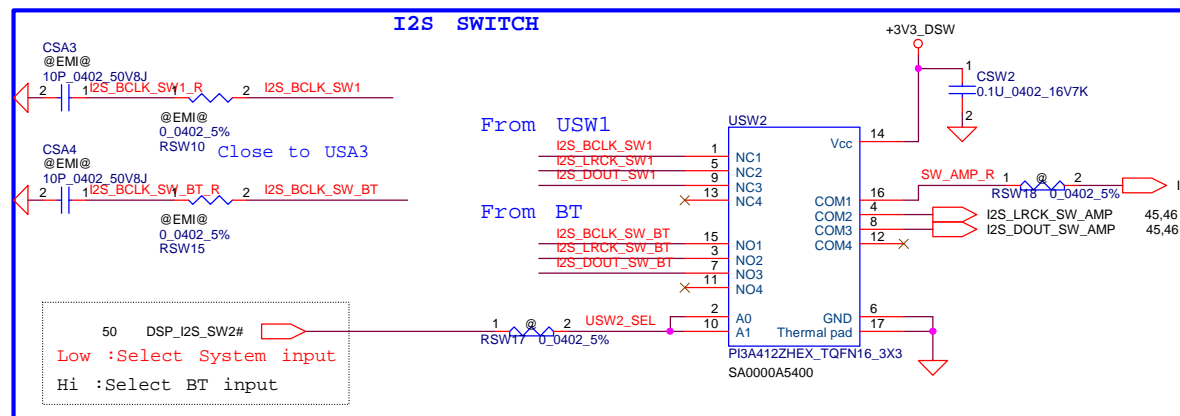
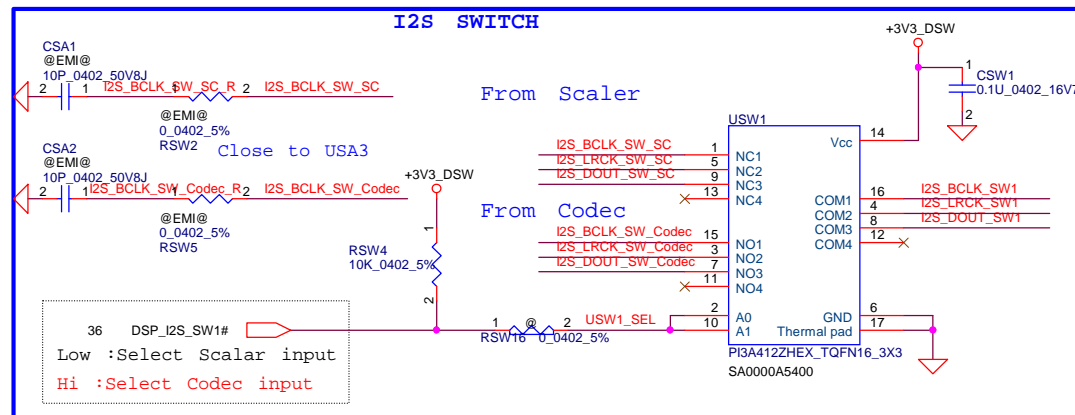
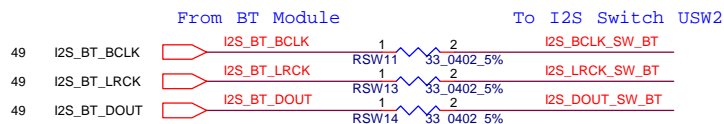
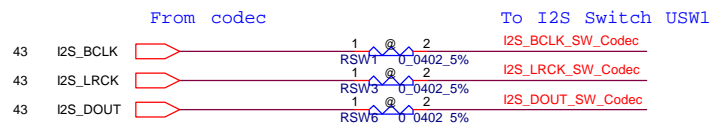
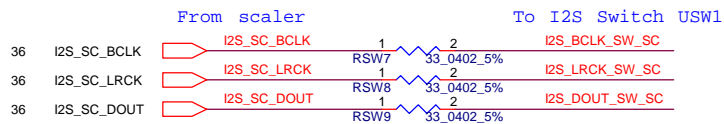






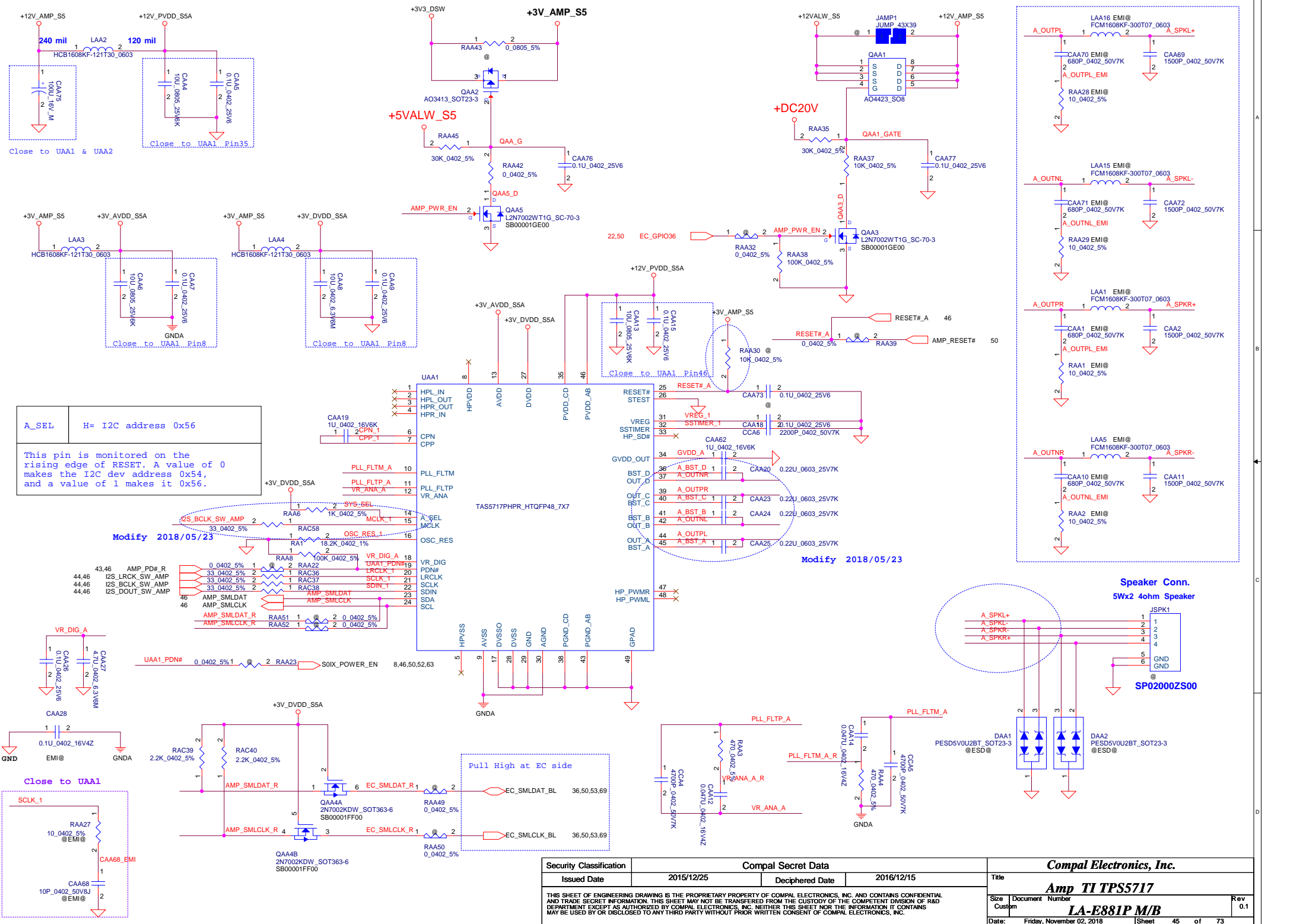


Security Classification		Compal Secret Data	
Issued Date	2015/12/25	Deciphered Date	2016/09/24
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		<b>Compal Electronics, Inc.</b> <b>HD Audio Codec ALC233</b> Size: 0.1 Document Number: LA-E822P M/B Date: Friday, November 02, 2018 13:43 of 73	



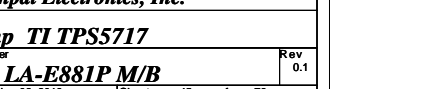
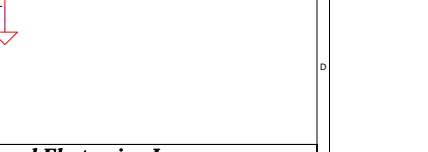
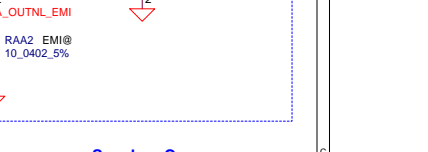
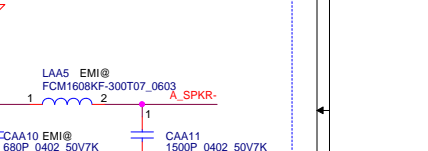
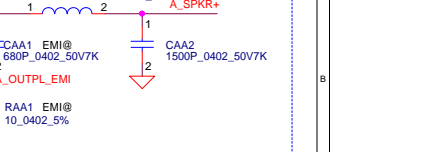
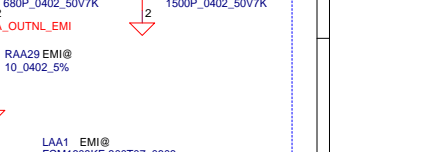
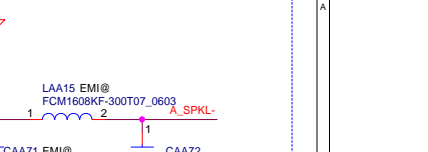
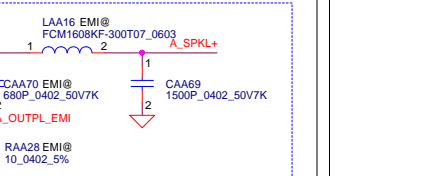
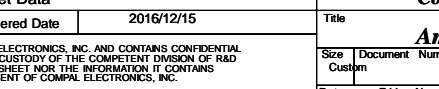
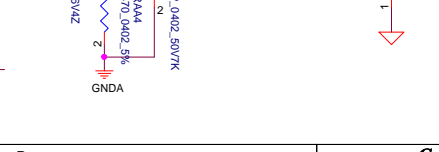
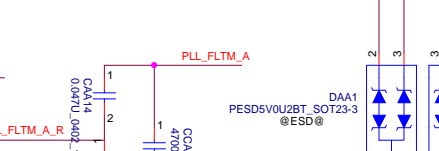
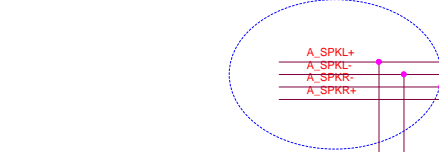
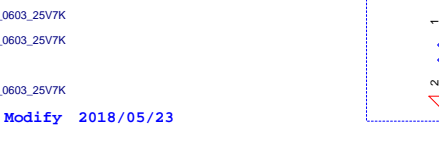
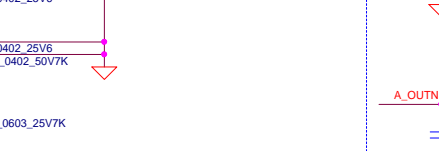
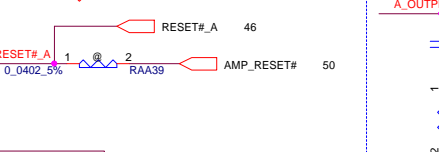
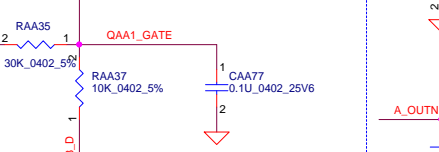
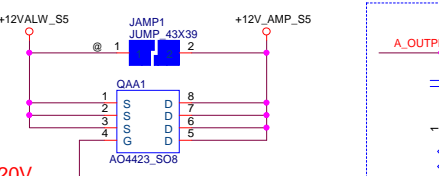
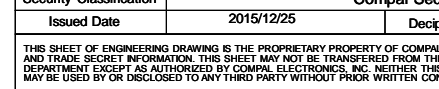
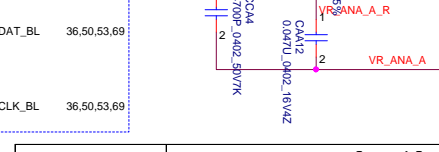
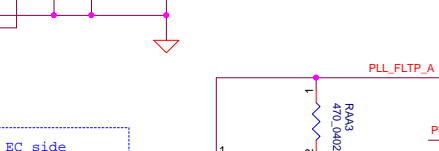
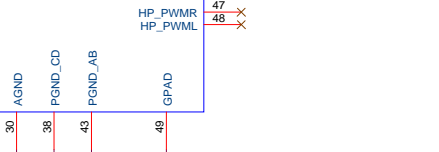
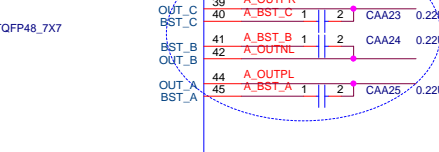
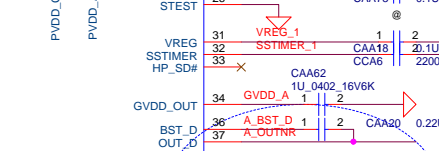
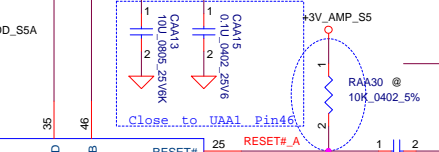
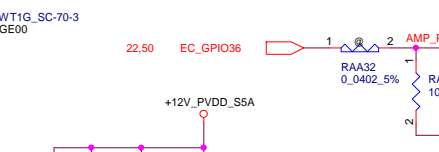
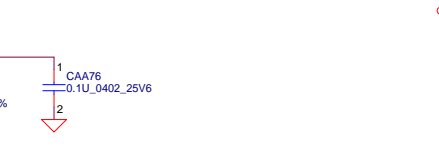
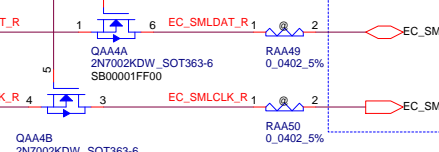
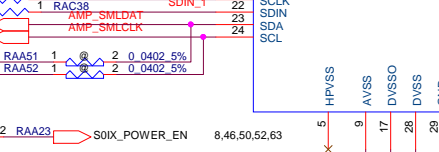
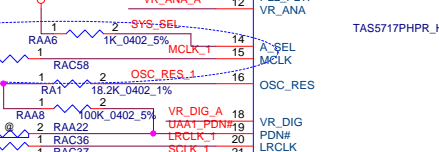
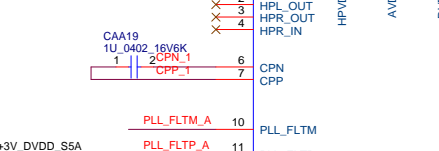
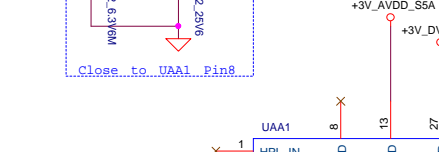
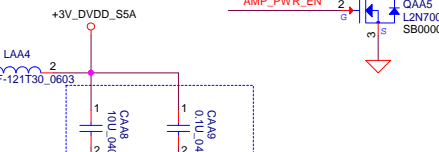
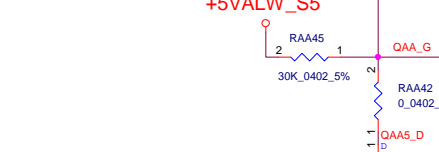
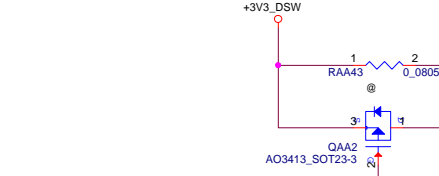
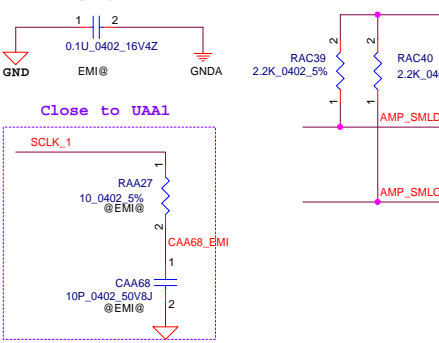
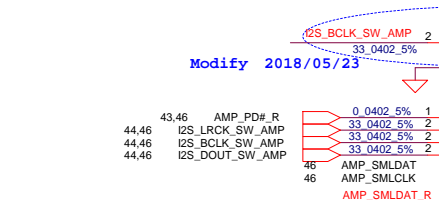
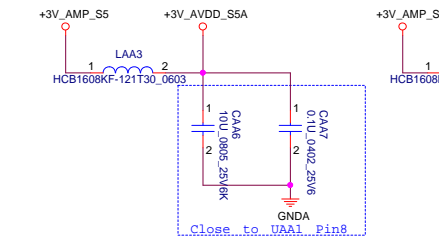
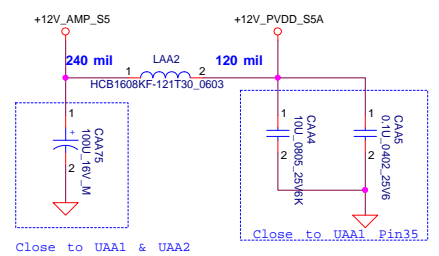
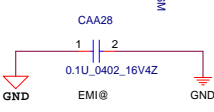
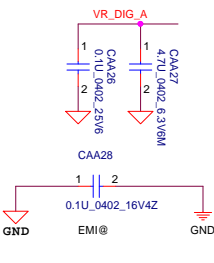
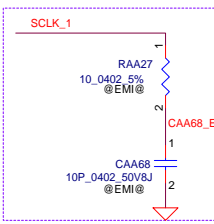
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2014/12/15		Deciphered Date		2016/12/15		Title	
										SMART AMP TAS5766MRMTR	
										C7 AIO-530	
										Rev 0.1	
										Date: Friday, November 02, 2018	
										Sheet 44 of 73	

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

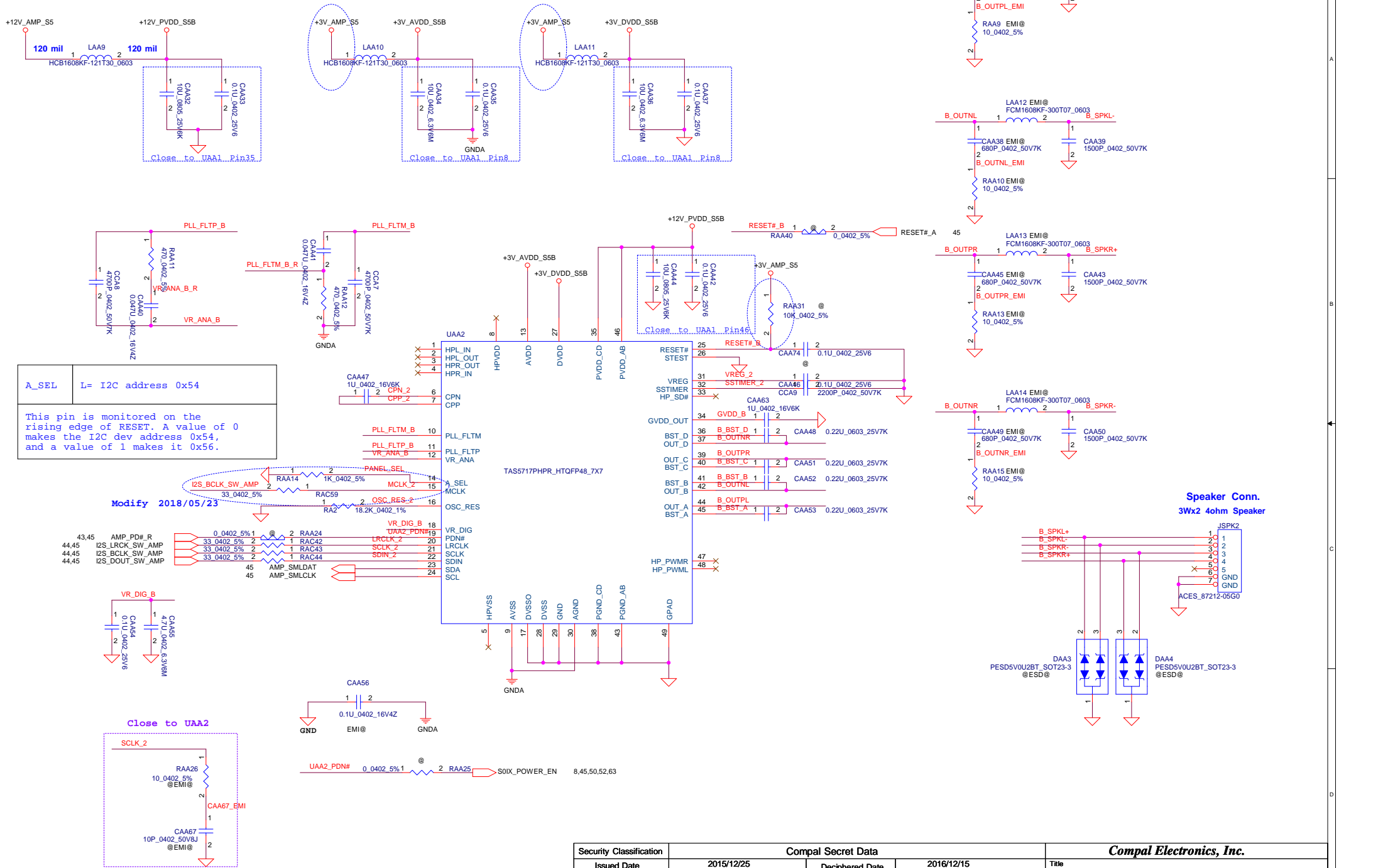


A\_SEL H= I2C address 0x56

This pin is monitored on the rising edge of RESET. A value of 0 makes the I2C dev address 0x54, and a value of 1 makes it 0x56.



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2016/12/15	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Amp TI TP55717
				Size Document Number
				Custom LA-E881P M/B
				Rev 0.1
				Date: Friday, November 02, 2018
				Sheet 45 of 73



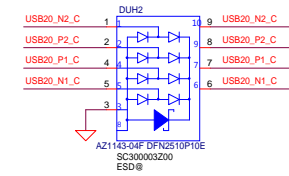
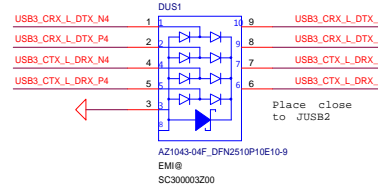
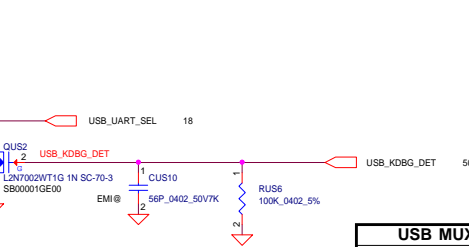
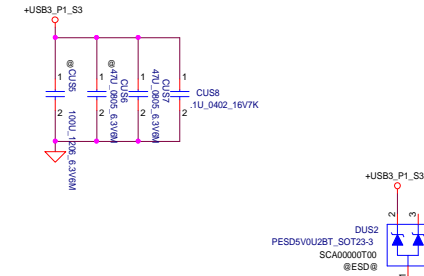
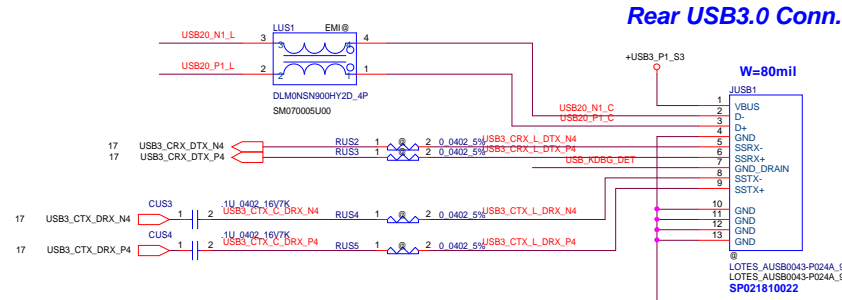
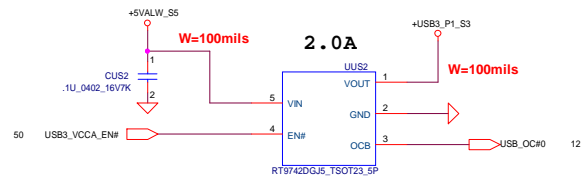
A\_SEL L= I2C address 0x54

This pin is monitored on the rising edge of RESET. A value of 0 makes the I2C dev address 0x54, and a value of 1 makes it 0x56.

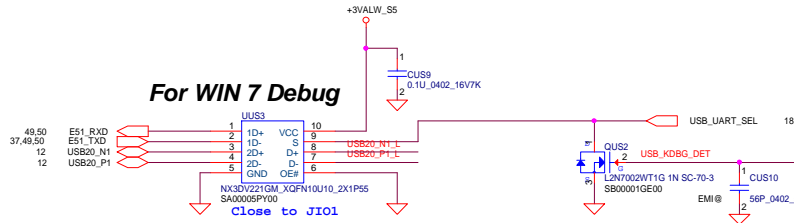
Modify 2018/05/23

Speaker Conn.  
3Wx2 4ohm Speaker

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2015/12/25		2016/12/15		Amp ANPEC APA6003	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size		Rev	
		Document Number		0.1	
		IA-E881P M/B			
Date:		Friday, November 02, 2018		Sheet 46 of 73	

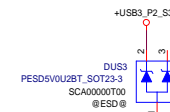
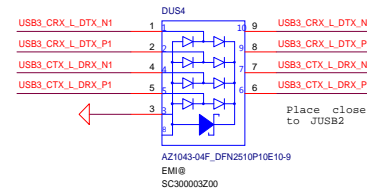
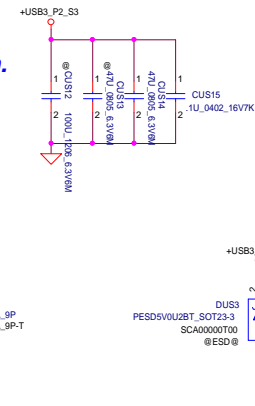
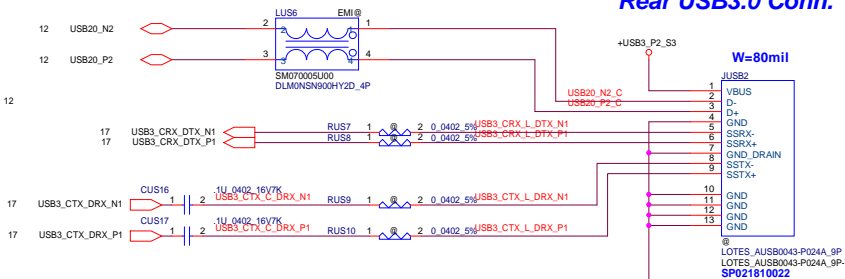
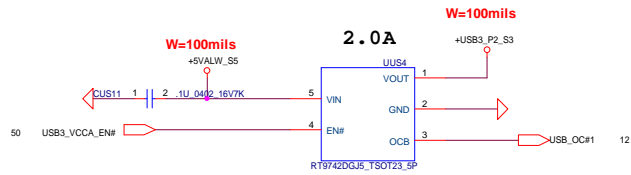


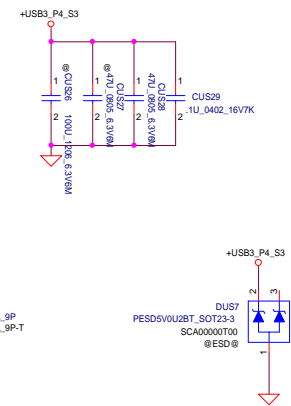
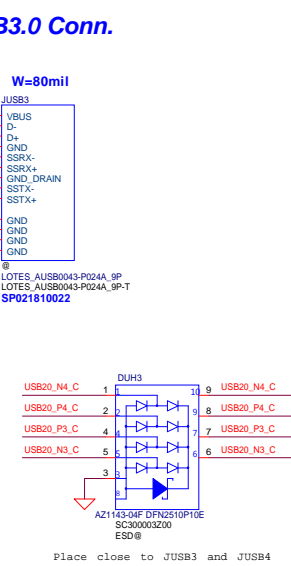
For WIN 7 Debug



USB_MUX Selection	
KDBG_MUX_SEL	Output
H	D = D2
L	D = D1

Rear USB3.0 Conn.

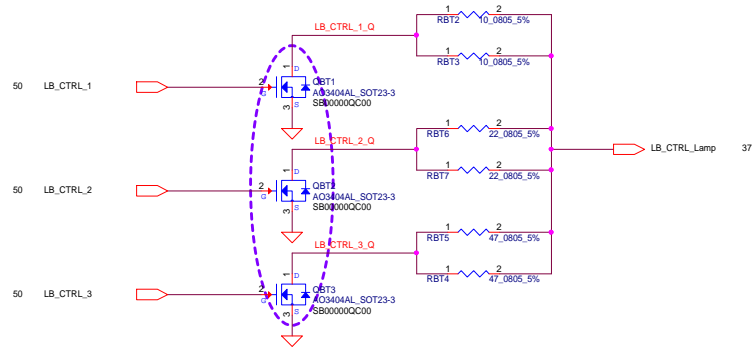




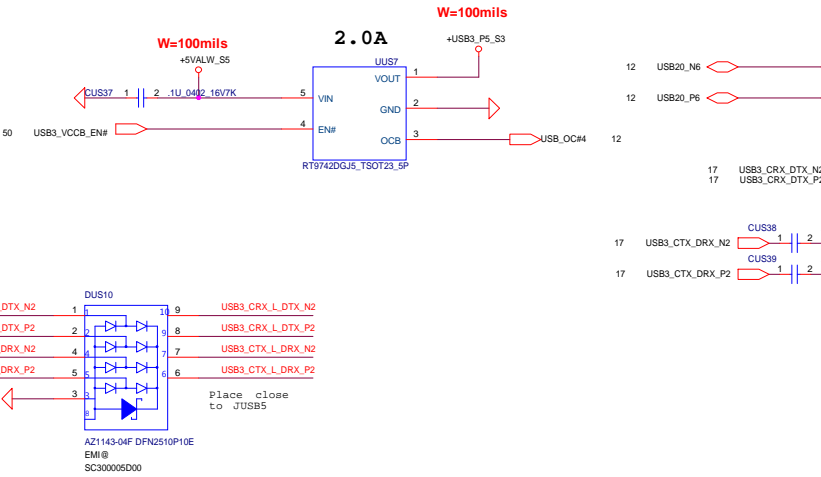
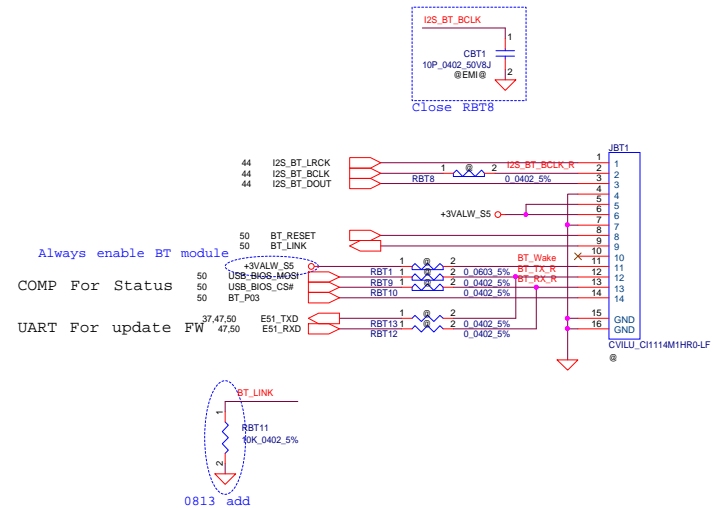
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Side USB3.0 x 2		
				Size C	Document Number	Rev 0.1
				LA-E881P M/B		
Date: Friday, November 02, 2016				Sheet	48	of 73



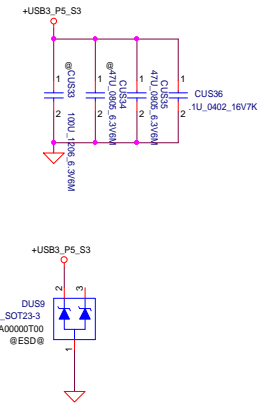
## Lamp control



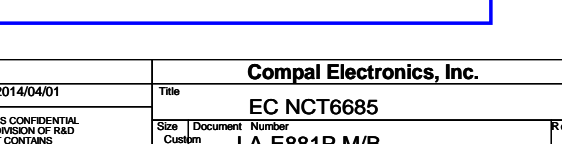
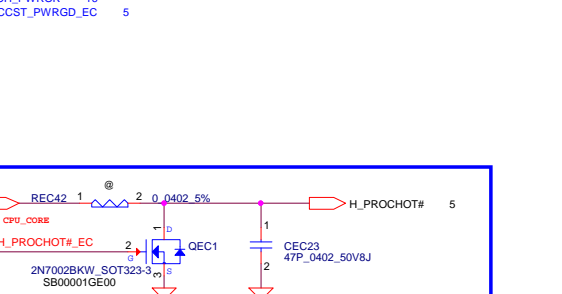
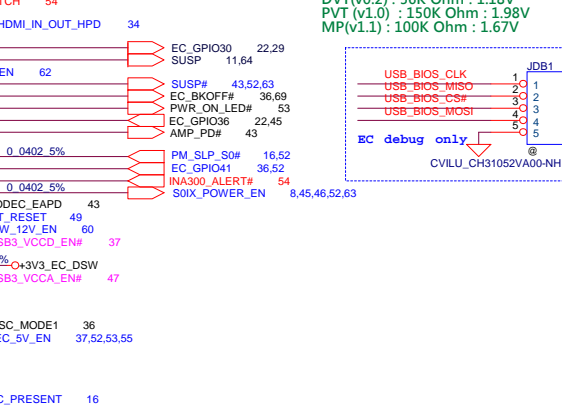
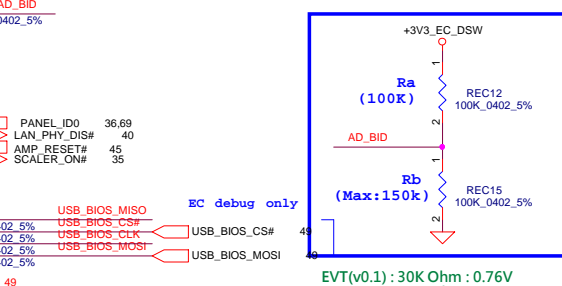
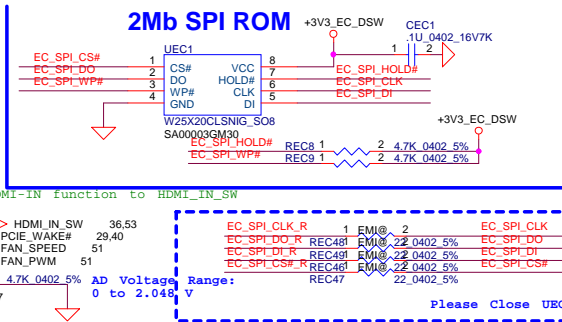
## To BT module



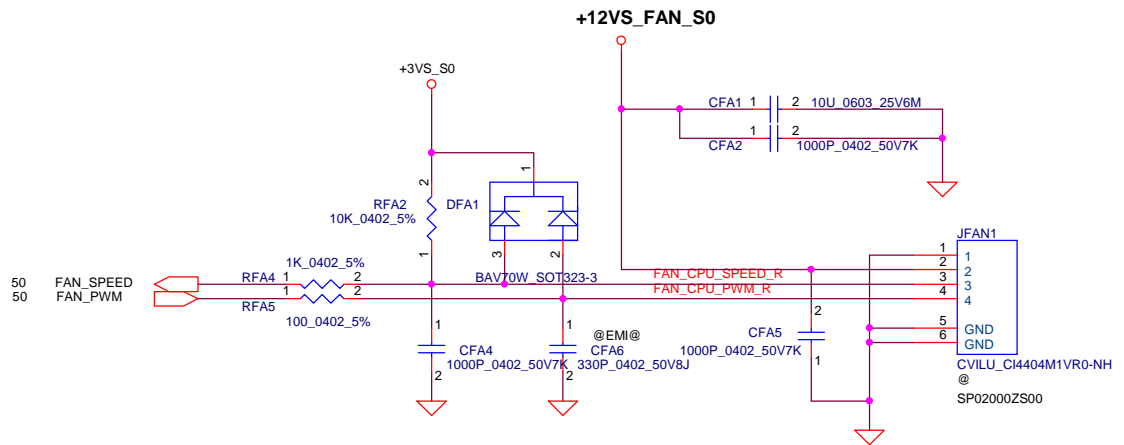
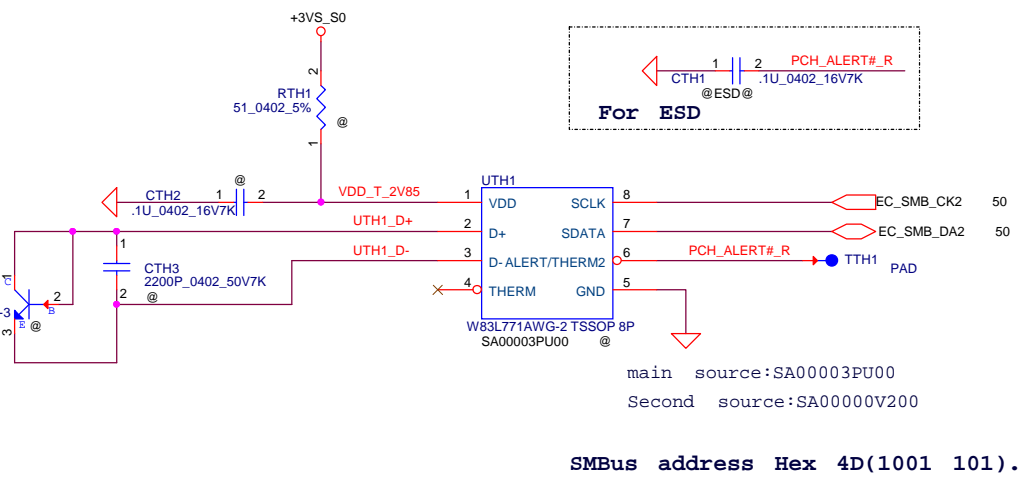
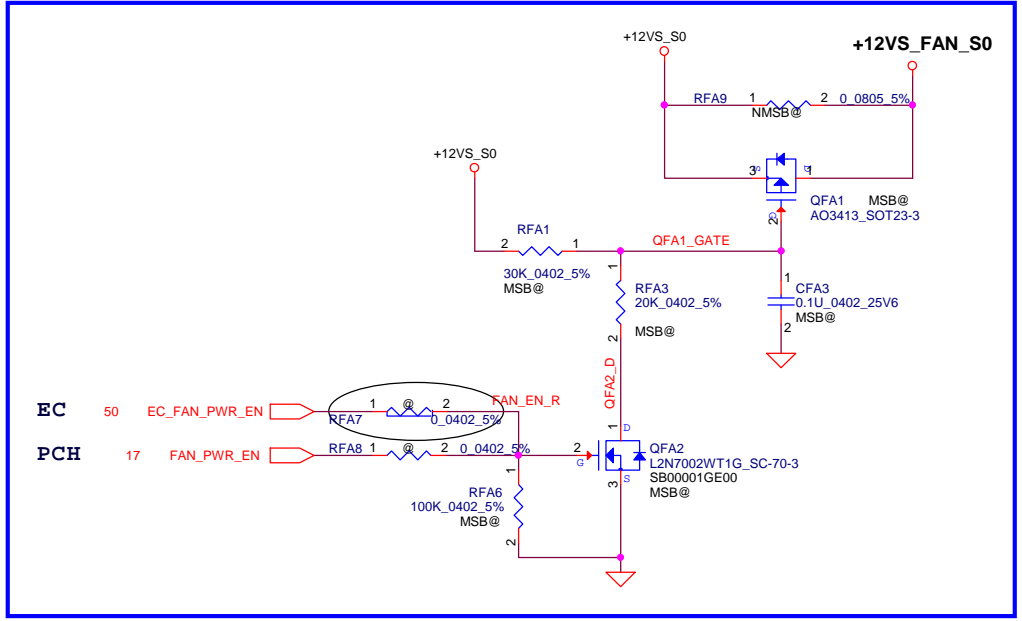
## Side USB3.1 Gen 2 Conn.



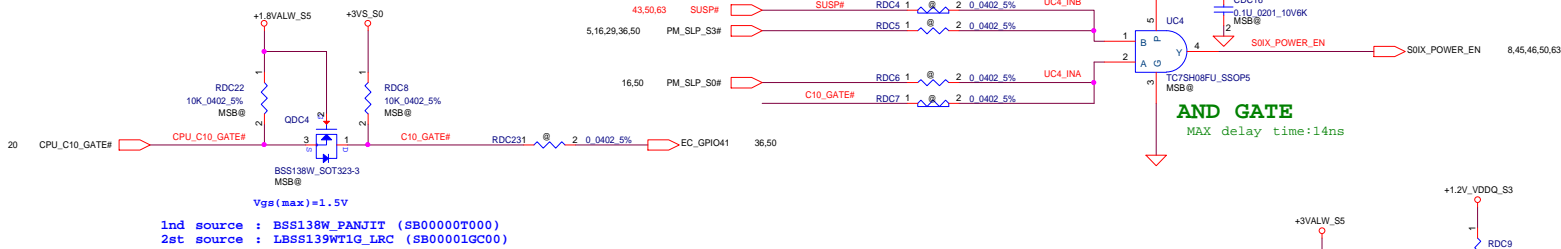
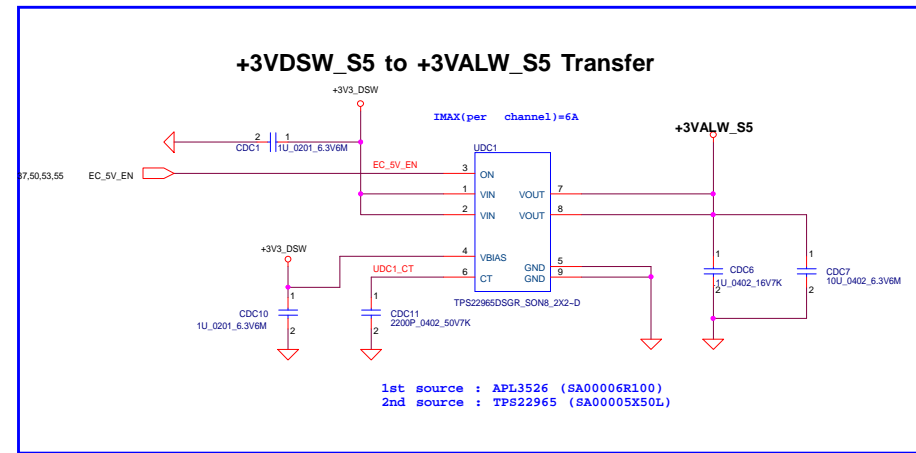
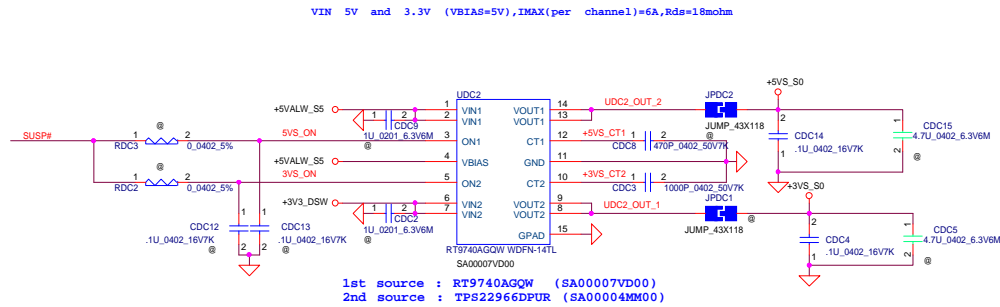
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2015/12/25	Deciphered Date		2016/09/24
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title	
				Side USB3.0 x 2	
				Document Number	
				LA-E881P M/B	Rev 0.1
				Date:	Friday, November 02, 2018
				Sheet	49 of 73



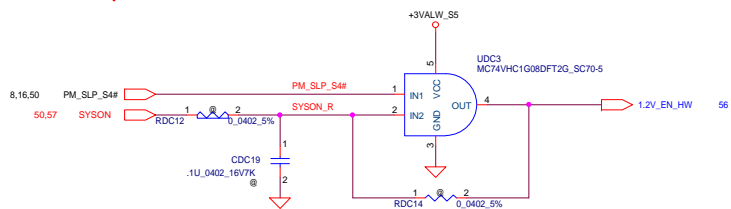
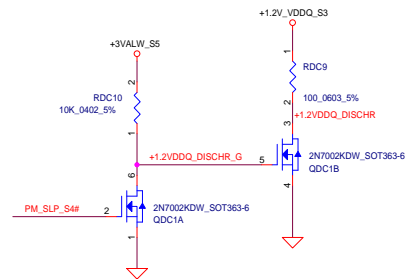
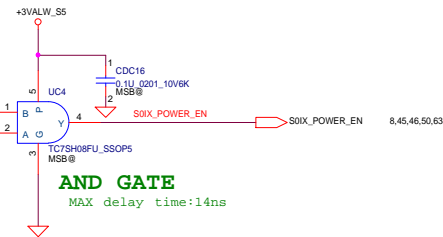
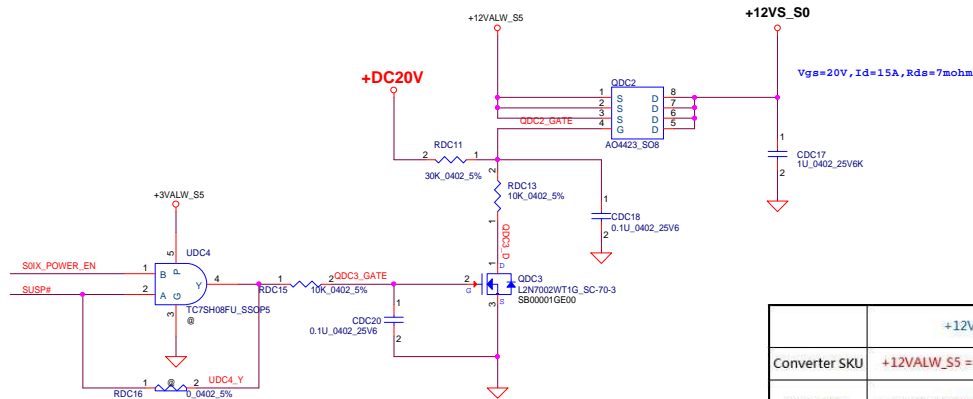
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2015/12/25	Deciphered Date	2014/04/01	EC NCT6685		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title		
				Size Document Number		
				Rev		
				Custom	LA-E881P M/B	0.1
				Date:	Friday, November 02, 2018	Sheet 50 of 73



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2015/10/02	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				FAN/Thermal Sensor	
Size		Document Number		Rev	
Date:		Friday, November 02, 2018		Sheet 51 of 73	



### +12VALW\_S5 TO +12VS\_S0 (PMOS)

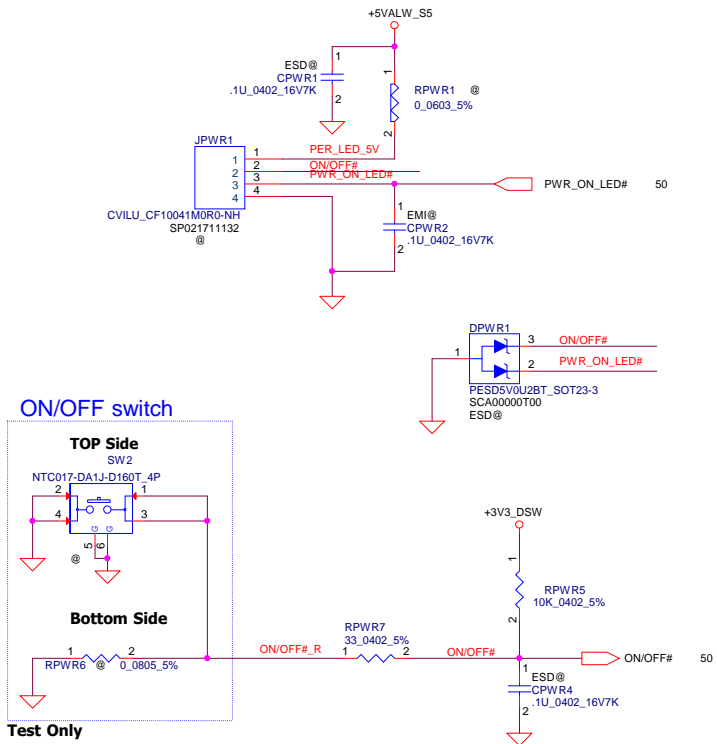


	+12VALW_S5	+12VS_S0	BOM
Converter SKU	+12VALW_S5 = +12VS_S0 ; Enable: HW_12V_EN# (Follow SPL_S3#)		RDC7,RDC8,RDC9
Scalar SKU	HW_12V_EN#(Follow SCALAR_ON#)	SUSP# (Follow SPL_S3#)	QDC2,RDC10,RDC16,RDC17,CDC19,CDC17

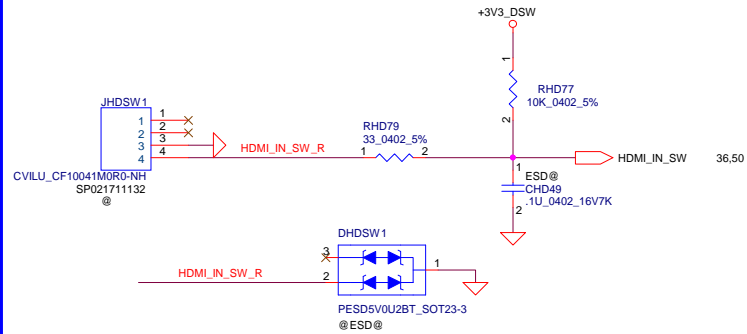
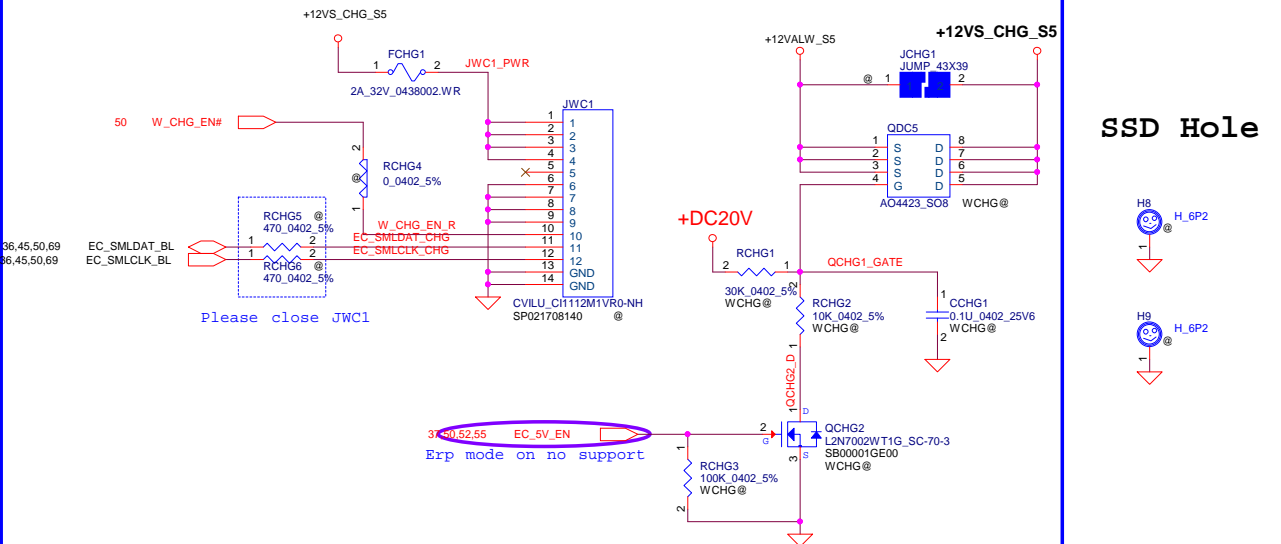
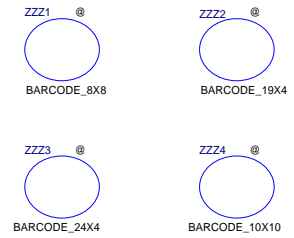
www.teknisi-indonesia.com

Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2015/12/25	DC INTERFACE
Deciphered Date	2016/03/27	LA-E881P M/B
Size	C	Rev 0.1
Date:	Friday, November 02, 2018	Sheet 52 of 73

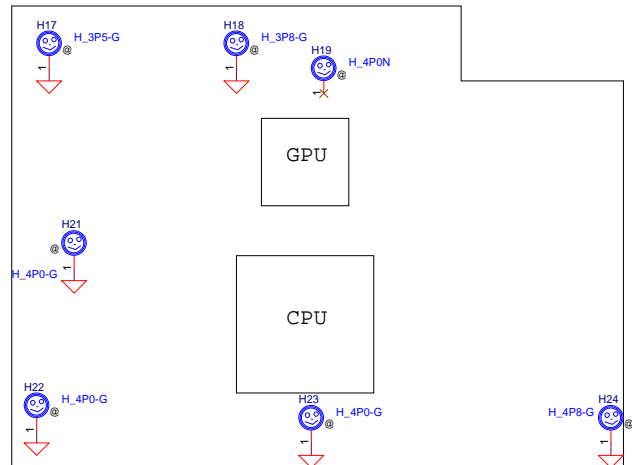
## Power Button



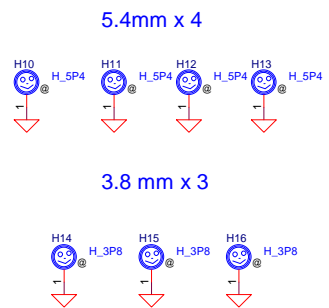
### ***HDMI Button board***

**BARCODE**

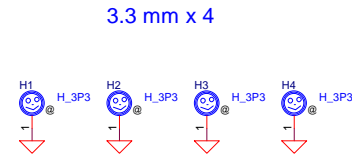
**Screw Hole**      5.4mm x 2      4.0 mm x 11



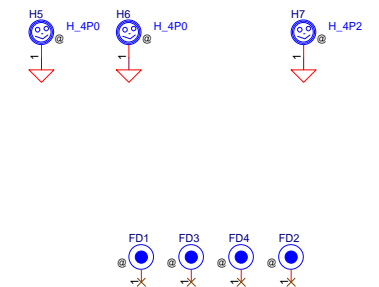
## CPU Hole



## GPU Hole



**Speaker**

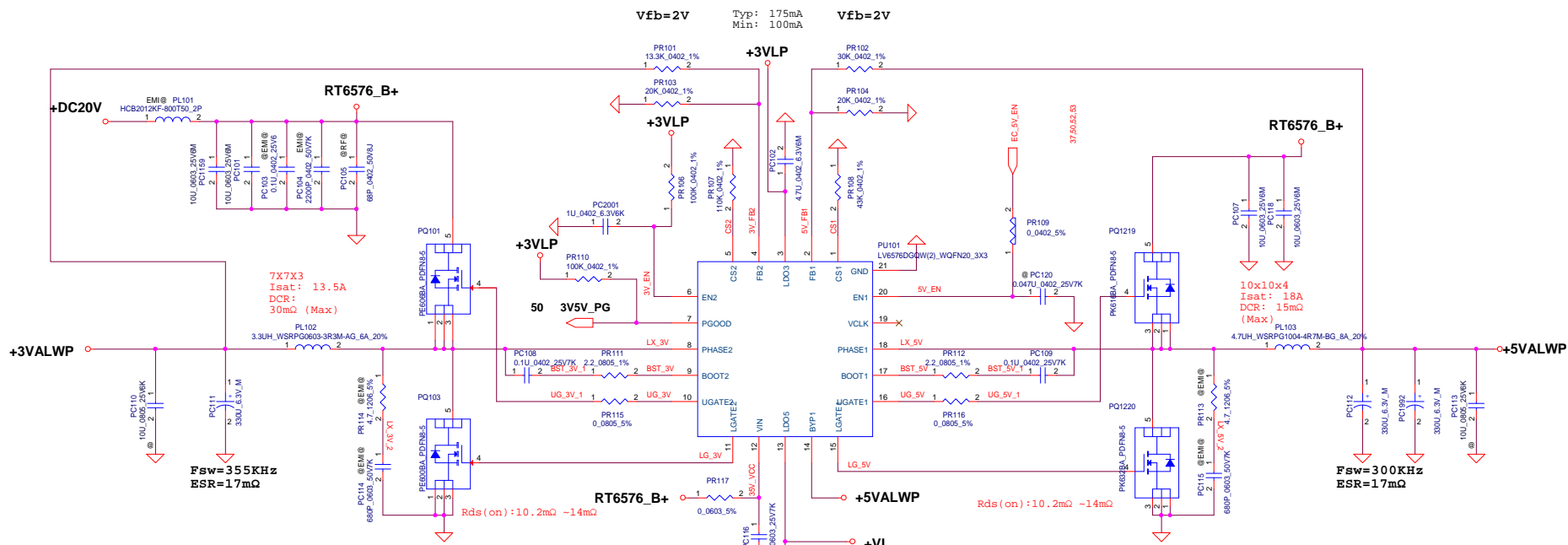


**FAN**

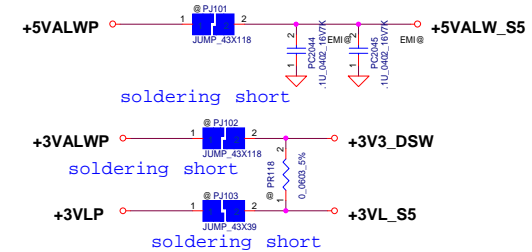
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>PWR SW/LED/SCREW</b>	
Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Document Number	0.1
				<b>LA-E881P M/B</b>	
Date: Friday, November 02, 2018				Sheet	53 of 73







main source : RT6576D  
second source:TPS51275B-1



+3VALWP  
Vin = 20V  
Iin = 3.3\*6.8/0.85/20  
= 1.32A

Vout = Vfb\*[1+(Rt/Rb)]  
= 2\*[1+(13.3K/20K)]  
= 3.3V

+5VALWP  
Vin = 20V  
Iin = 5\*10.76/0.85/20  
= 3.16A

Vout = Vfb\*[1+(Rt/Rb)]  
= 2\*[1+(30K/20K)]  
= 5V

+3VALWP  
Imax=4.9A ; Ipeak=7A ; Fsw=355KHz  
Iocp=(Rcs1\*Itrip)/(8\*Rdson)  
Rds : L/S --> typ:10.2mohm ; max: 14mohm  
Itrip=9~11 uA  
Iocp(set)=10A~13.5A  
Iin\_ripple=1.66A  
Output Cap. ESR=17mohm  
Delta IL=[(Vin-Vo)/L]\*[(Vout/Vin)\*T]=2.352A  
LIR=Delta IL/Ipeak=0.367  
Cout=[L\*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]  
=240.02uF  
CINBULK=Iload\*Vout\*(Vin-Vout)/(Fsw\*Vin^2\*VINPP)=0.87uF

+5VALWP  
Imax=7.53A, Ipeak=10.76A ; Fsw=300KHz  
Iocp=(Rcs1\*Itrip)/(8\*Rdson)  
Rds : L/S --> typ:3 ohm ; max: 4mohm  
Itrip=9~11 uA  
Iocp(set)=17.2A~21A  
Iin\_ripple=2.56A  
Output Cap. ESR=17mohm  
Delta IL=[(Vin-Vo)/L]\*[(Vout/Vin)\*T]=2.660A  
LIR=Delta IL/Ipeak=0.315  
Cout=[L\*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]  
=243.73uF  
CINBULK=Iload\*Vout\*(Vin-Vout)/(Fsw\*Vin^2\*VINPP)=1.85uF

main source : RT8207MZQW  
second source:UP1566PQKF

+0.6VSP  
TDC=0.42A  
Ipeak=0.6A

V <sub>o</sub>	0.6	
V <sub>in</sub>	1.2	
I <sub>o</sub>	0.75	
PD	0.455	
θ JA(main)	52	° C/W
θ JA(2nd)	68	

RT8207M:  
Quiescent Current (GND Current)  
I<sub>Q</sub>(typ)=0.47mA, I<sub>Q</sub>(max)=1mA  
PD=(V<sub>in</sub>-V<sub>out</sub>)\*I<sub>out</sub> + V<sub>in</sub>\*I<sub>Q</sub> =0.455W  
θ JA= 33.7° C/W\*0.903=23.66°C

Mode Level +0.6VSP VTTREF\_1.2V  
S3 L off off  
S3 L off on  
S0 H on on  
Note: S3 - sleep ; S5 - power off

+1.2VP  
V<sub>in</sub> = 20V  
I<sub>in</sub> = 7.3\*1.2/0.85/20  
= 0.51A

V<sub>out</sub> = V<sub>fb</sub>\*[1+(R<sub>t</sub>/R<sub>b</sub>)]  
= 0.75\*[1+(6.04K/10K)]  
= 1.203V

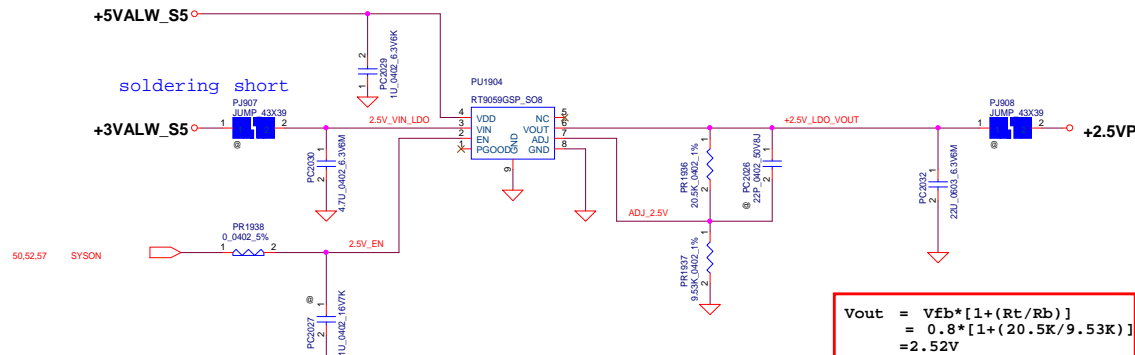
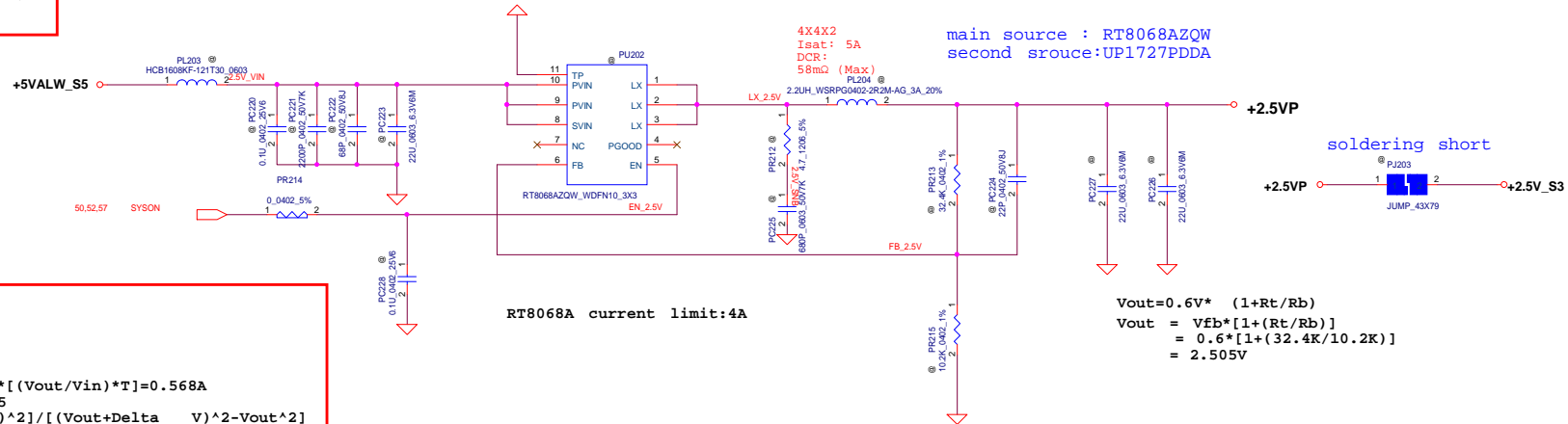
+1.2VP  
I<sub>max</sub>=5.4A ; I<sub>peak</sub>=7.7A ; F<sub>sw</sub>=285KHz  
I<sub>oqp</sub>=(R<sub>cs1</sub>\*I<sub>trip</sub>)/(8\*R<sub>ds(on)</sub>)  
R<sub>ds</sub> : 1/S --> typ:12.1mohm ; max: 14mohm  
I<sub>trip</sub>=9-11 uA  
I<sub>oqp</sub>(set)=11-14A  
I<sub>in\_ripple</sub>=1.21A  
Output Cap. ESR=17mohm  
Delta I<sub>L</sub>=[(V<sub>in</sub>-V<sub>o</sub>)/L]\*[(V<sub>out</sub>/V<sub>in</sub>)\*T]=1.799A  
LIR=Delta I<sub>L</sub>/I<sub>peak</sub>=0.246  
C<sub>out</sub>=[L\*(I<sub>out</sub>+Delta I<sub>L</sub>/2)\*2]/[(V<sub>out</sub>+Delta V)^2-V<sub>out</sub>^2]  
=676.16uF  
CINBULK=I<sub>load</sub>\*V<sub>out</sub>\*(V<sub>in</sub>-V<sub>out</sub>)/(F<sub>sw</sub>\*V<sub>in</sub>^2\*VINPP)=0.51uF

www.teknisi-indonesia.com

Security Classification	Compal Secret Data		Title	
Issued Date	2015/07/27	Deciphered Date	2016/07/27	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF HAD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				1.2VP/0.6VSP(RT8207M)
Size	Document	Number	Rev	0.1
Date:	Friday, November 02, 2018	Sheet	66	of 73

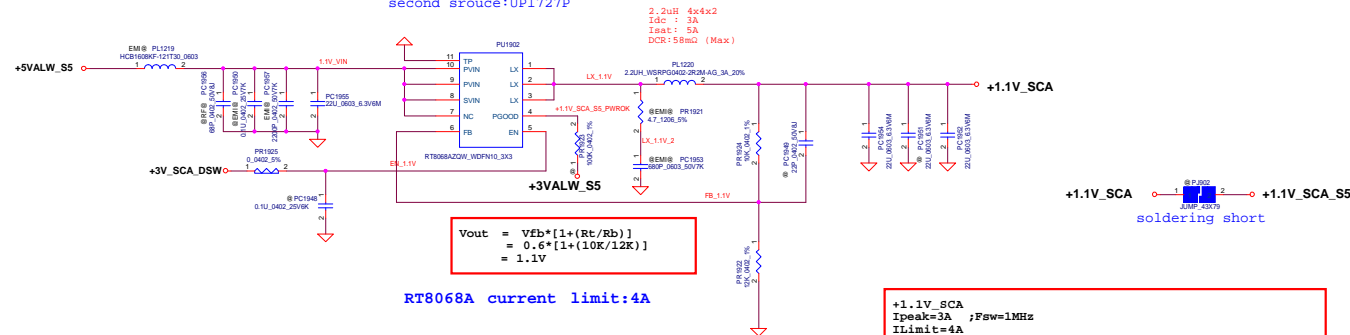
+2.5VP  
 $V_{in} = 5V$   
 $I_{in} = 2.5 \times 2.24 / 0.85 / 5$   
 $= 1.32A$

+2.5VP  
 $I_{peak} = 1.5A$  ;  $F_{sw} = 1MHz$   
 $I_{Llimit} = 4A$   
 $I_{in\_ripple} = 0.75A$   
 $\Delta I_L = [(V_{in} - V_o) / L] \times [(V_{out} / V_{in}) \times T] = 0.568A$   
 $LIR = \Delta I_L / I_{peak} = 0.25$   
 $C_{out} = [L \times (I_{out} + \Delta I_L / 2) \times 2] / [(V_{out} + \Delta V)^2 - V_{out}^2] = 11.8\mu F$   
 $CINBULK = I_{Load} \times V_{out} \times (V_{in} - V_{out}) / (F_{sw} \times V_{in}^2 \times VINPP) = 0.78\mu F$



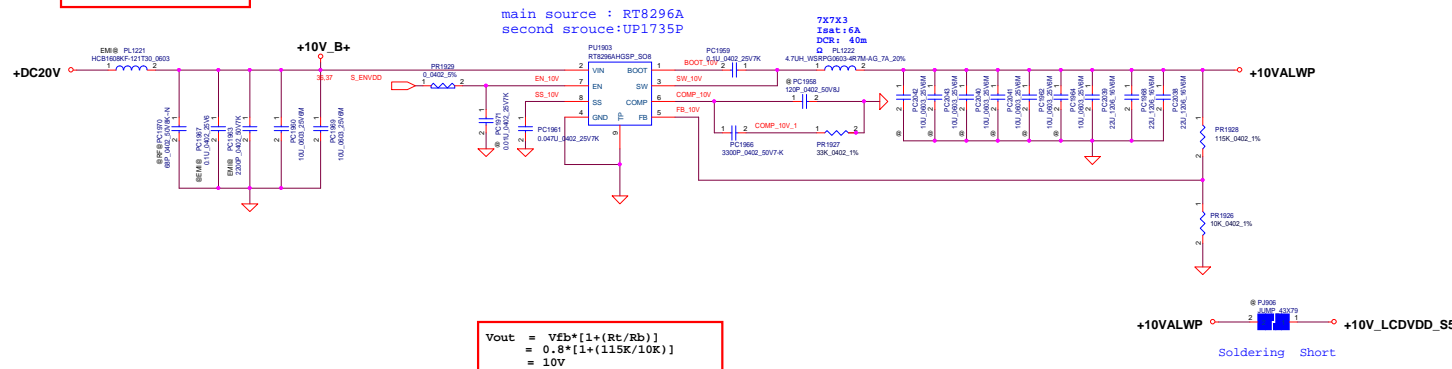
+1.1V\_SCA  
Vin =5V  
Iin =1.1\*1.94/0.9/5  
=0.58A

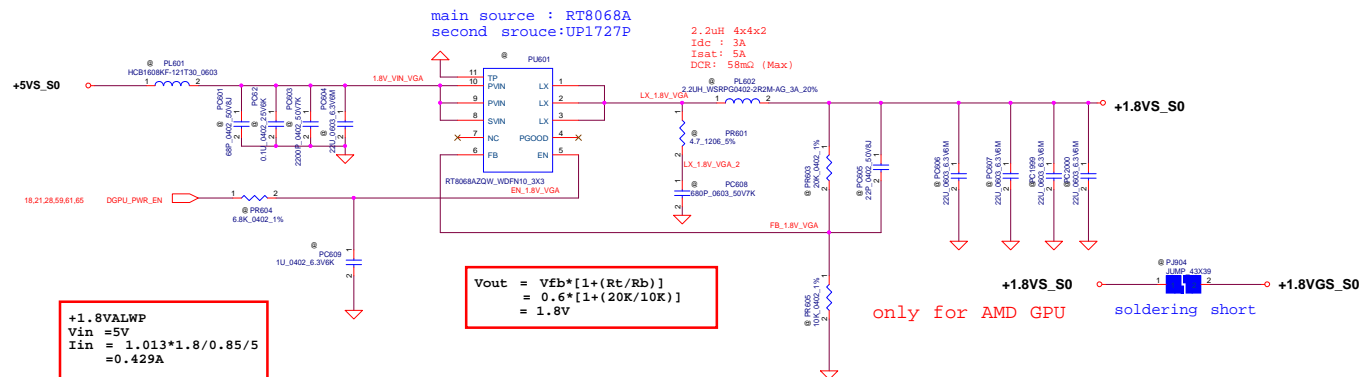
main source : RT8068A  
second source:UP1727P



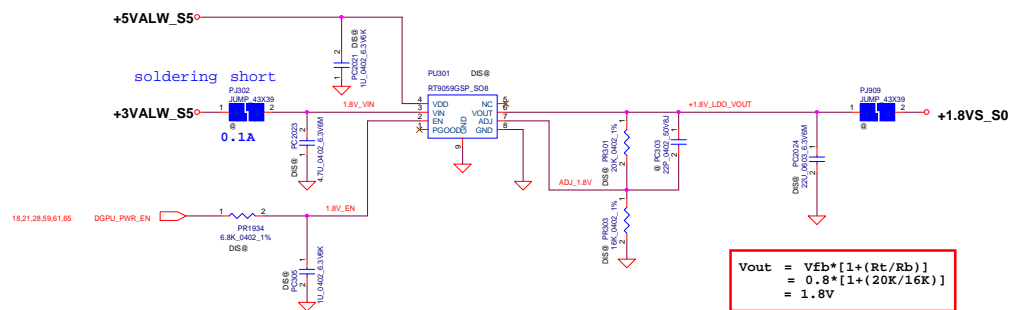
+10VALWP  
Vin =20V  
Iin = 10\*1.04/0.85/20  
=0.61A

main source : RT8296A  
second source:UP1735P





+1.8VALWP  
Ipeak=1.013A ;Fsw=1MHz  
ILimit=4A  
Tin\_ripple=0.4A  
Delta IL=[(Vin-Vo)/L]\*[(Vout/Vin)\*T]=0.745A  
LIR=Delta IL/Ipeak=0.372  
Cout=[L\*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]  
=20.81uF  
CINBULK=Iload\*Vout\*(Vin-Vout)/(Fsw\*Vin^2\*VINPP)=0.06uF

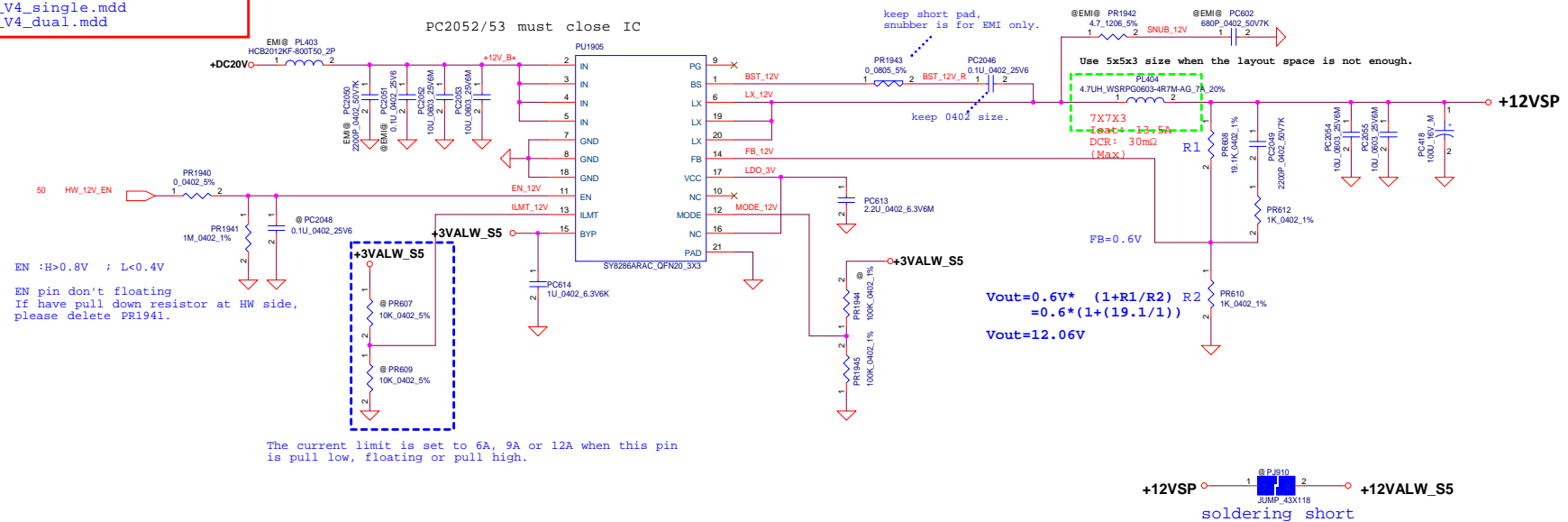


```
Module model information
SY8286_V4_single.mdd
SY8286_V4_dual.mdd
```

```
Module model information
SY8286_V4_single.mdd
SY8286_V4_dual.mdd
```

```
main source : SY8286A
second srouce:JW5069A
```

PC2052/53 must close IC



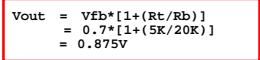
```
+12VSP
Imax=2.607,Ipeak=3.724A      ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/Rdsn
Rds : 1/S --> typ:12.1mohm ; max: 14mohm
Itrip=9-11 uA
Iocp(set)=10-13.5A
Iin_ripple=0.97A
Output Cap. ESR=24mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=3.404A
LIR=Delta IL/ILpeak=0.914
Iout=[L*(Iout+DeltaIL/2)*2]/[(Vout+Delta V)^2-Vout^2]
=15uF
CINBULK=ILOAD*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.04uF
```

$$\begin{aligned} V_{out} &= V_{fb} \cdot [1 + (R_t/R_b)] \\ &= 0.8 \cdot [1 + (2.1K/150)] \\ &= 12V \end{aligned}$$

```
+12VSP
Vin = 20V
Iin = 12*2.1/0.85/20
     = 2.63A
```



```
+0.875V
Vin = 20V
Iin = 8*0.875/0.85/20
     = 0.412A
```



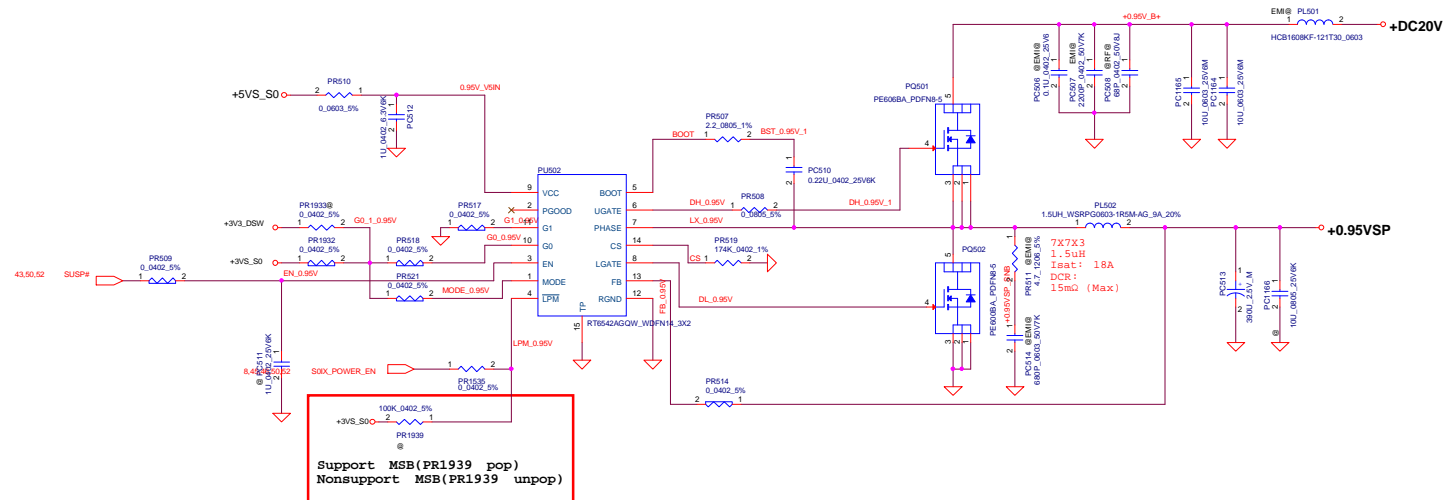
Security Classification	Compul Secret Data		Title		Rev 0.1
Issued Date	2013/08/29	Deciphered Date	2013/08/29	0.875W(TPS51212)	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPUL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND PROPRIETARY INFORMATION. THIS SHEET MUST NOT BE LOANED, REPRODUCED, COPIED, OR DISCLOSED TO ANY OTHER PERSON OR ENTITY WITHOUT THE WRITTEN CONSENT OF COMPUL ELECTRONICS, INC. THE COMPANY DIVISION OF READ DEPARTMENT EXCEPT AS AUTHORIZED BY COMPUL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPUL ELECTRONICS, INC.</p>				Size Date	Docu Date
				Fri, Nov 08, 2013	Sheet 61 of 73

$$\begin{aligned} V_{out} &= V_{fb} * [1 + (R_t / R_b)] \\ &= 0.7 * [1 + (5K / 10K)] \\ &= 1.05V \end{aligned}$$

$\Delta I_L / I_{peak} = 0.203$   
 $\Delta t = [I * (I_{out} + \Delta I_L / 2)^2] / [(V_{in} - V_{out})^2]$   
 $\Delta t = 46.12 \mu F$   
 $I_{BULK} = I_{load} * V_{out} * (V_{in} - V_{out}) / (F_{sw} * V_{in}^2 * 2 * V_{INPP}) = 0.46 \mu F$

FB = 0.7v  
 main source : TPS51212DSCR  
 second source: RT8237EZQW  
 Rds(on): 10.2mΩ ~14mΩ

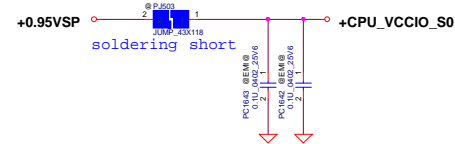
Security Classification		Compal Secret Data		Title	
Issued Date	2013/08/29	Deciphered Date	2013/08/29	<b>VPCH1.05V(TPS51212)</b> Size      Document      Number	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED, REPRODUCED, COPIED, OR DISCLOSED TO ANY OTHER PERSON OR ENTITY WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC. IF YOU ARE AN EMPLOYEE OF COMPAL ELECTRONICS, INC. YOU MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date:	Friday, November 02, 2018 Sheet      62      of      73



+0.95VSP  
 $I_{max}=4.48A, I_{peak}=6.4A ; F_{sw}=290KHz$   
 $I_{ocp}=(R_{cs1} \cdot I_{trip})/R_{dson}$   
 $R_{ds} : L/S \rightarrow typ:10.2m\Omega ; max: 14m\Omega$   
 $I_{trip}=9-11 \mu A$   
 $I_{ocp(set)}=11.3-13.59A$   
 $I_{in\_ripple}=1.24A$   
 $Output\ Cap. ESR=17m\Omega$   
 $\Delta IL=[(V_{in}-V_o)/L] \cdot [(V_{out}/V_{in}) \cdot T]=2.08A$   
 $LIR=\Delta IL / I_{peak}=0.249$   
 $C_{out}=[L \cdot (I_{out}+\Delta IL/2)^2] / [(V_{out}+\Delta V)^2 - V_{out}^2]$   
 $=1293.74\mu F$   
 $CINBULK=I_{Load} \cdot V_{out} \cdot (V_{in}-V_{out}) / (F_{sw} \cdot V_{in}^2 \cdot VINPP)=0.46\mu F$

+0.95VSP  
 $V_{in} = 20V$   
 $I_{in} = 0.95 \cdot 8.35 / 0.85 / 20$   
 $= 0.466A$

$V_{out} = V_{fb} \cdot [1 + (R_t/R_b)]$   
 $= 0.7 \cdot [1 + (5K/14.3K)]$   
 $= 0.95V$



teknisi-indonesia.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/08/29	Deciphered Date	2013/08/29	Title	VCCIO 0.95V(TPS51212)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Date	Friday, November 02, 2018
				Sheet	63 of 73
				Rev	0.1

$$V_{out} = V_{fb} * [1 + (R_t / R_b)]$$

$$= 0.8 * [1 + (9.53K / 30K)]$$

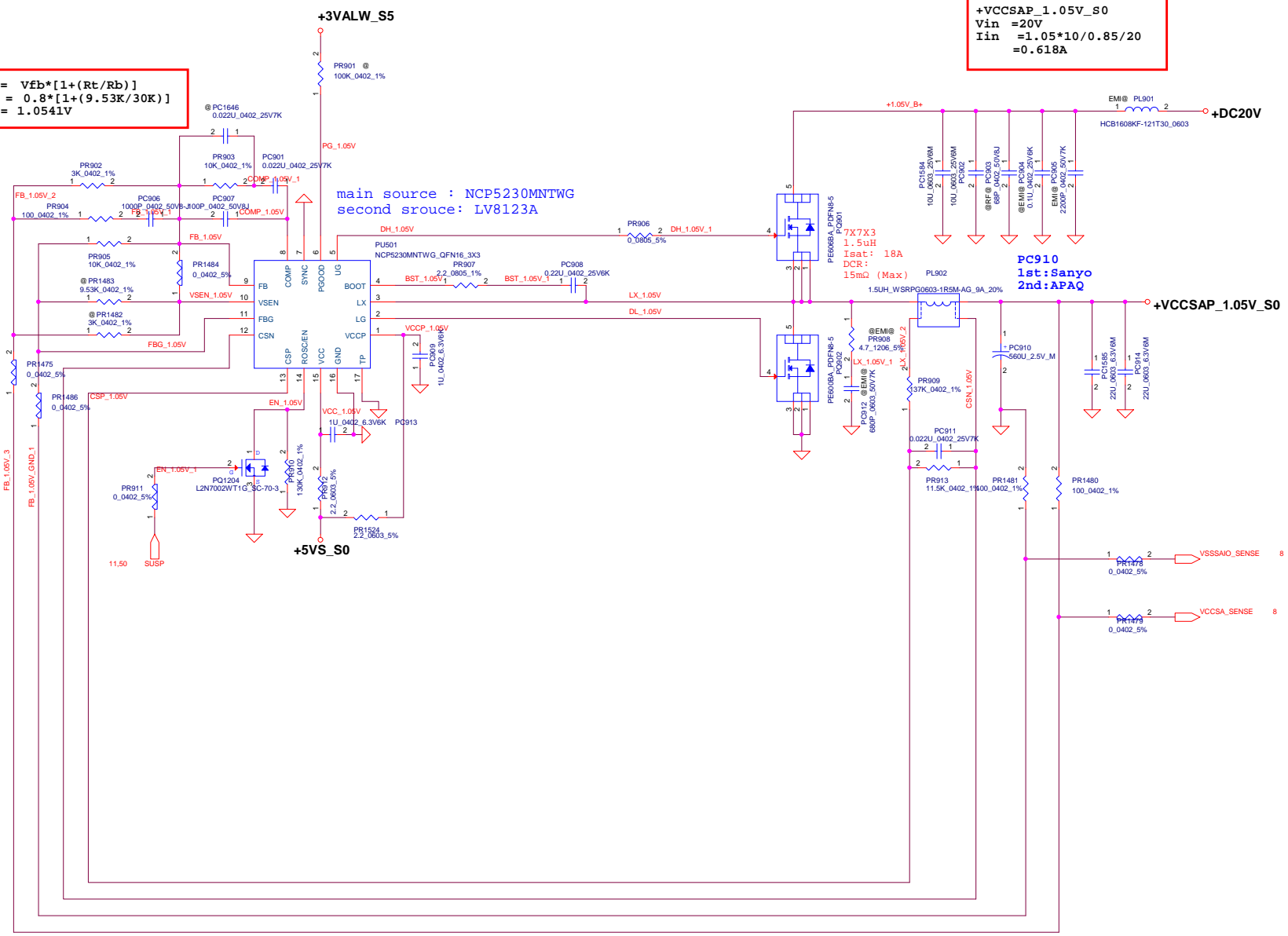
$$= 1.0541V$$

$$+VCCSAP\_1.05V\_S0$$

$$V_{in} = 20V$$

$$I_{in} = 1.05 * 10 / 0.85 / 20$$

$$= 0.618A$$

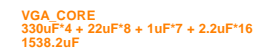
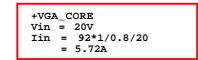


+1.05VSP  
 $I_{max} = 7.826A$ ,  $I_{peak} = 11.18A$  ;  $F_{sw} = 300KHz$   
 $I_{ocp} = (R_{cs1} * I_{trip}) / R_{dson}$   
 $R_{ds} : L/S \rightarrow typ: 11mohm ; max: 17.5mohm$

$I_{ocp}(set) : \sim 17.2A$   
 $I_{in\_ripple} = 1.72A$   
 Output Cap.  $ESR = 9mohm$   
 $\Delta IL = [(V_{in} - V_o) / L] * [(V_{out} / V_{in}) * T] = 2.21A$   
 $\Delta I_{IR} = \Delta IL / I_{peak} = 0.201$   
 $C_{out} = [L * (I_{out} + \Delta IL / 2)^2] / [(V_{out} + \Delta V)^2 - V_{out}^2]$   
 $= 1029.17\mu F$   
 $CINBULK = I_{Load} * V_{out} * (V_{in} - V_{out}) / (F_{sw} * V_{in}^2 * VINPP) = 0.64\mu F$

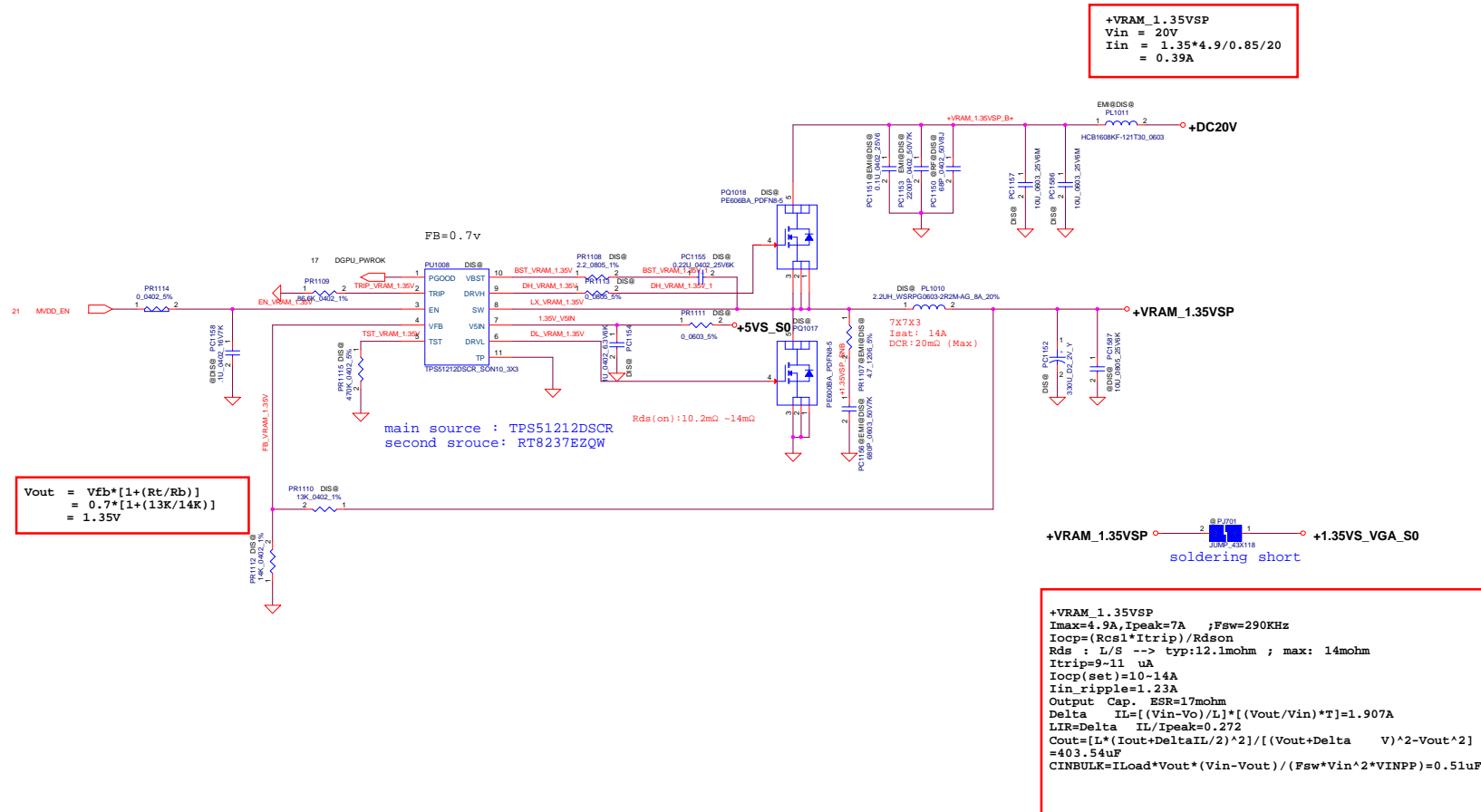
+VCCSAP\_1.05V\_S0 @ PJ901  
 JUMP\_43X118  
 soldering short +1.05VS\_VCCSA\_S0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/08/29	Deciphered Date	2013/08/29	Title	VCCSA_1.05VSP(NCP5230M)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	Rev 1.0
				Date:	Friday, November 02, 2018
				Sheet	64 of 73



```
+VGA_CORE [AMD R17M-G1-50]
TDC=38A; Ipeak=70A; Iocp>=90A
Fsw=400K
Inductor DCR=0.82mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm; max: 7mohm
L/S --> typ: 2.1mohm; max: 3.3mohm
Delta IL=(Vin-Vout)/[I*(Vout/Vin)]=8.727A
LIIR=Delta LI/Ipeak=0.388
Count=[L*(Vout+DeltaLI/2)*2]/((Vout+Delta V)^2-Vout^2)
=1356.75uf
CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.76uF
```

Security Classification	Compul Secret Data		Ttn		Compul Electronics, Inc.	
Issued Date	2013/06/29	Deciphered Date	2013/06/29	VGA CORE(RT8880C)		
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPUL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. THIS SHEET OF ENGINEERING DRAWING IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS WITHOUT THE WRITTEN PERMISSION OF COMPUL ELECTRONICS, INC. THE INFORMATION ON THIS SHEET OF ENGINEERING DRAWING IS NOT TO BE USED FOR ANY OTHER PURPOSES THAN THE DESIGN OF COMPUL ELECTRONICS, INC. PRODUCTS.</p>				Rev	0.1	
<p>Date: Friday, November 02, 2018</p>				Sheet	65	of 73



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/08/29	Deciphered Date	2013/08/29	Title	<b>VRAM_1.35V(TPS51212)</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMMENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Rev 0.1
				Date	Friday, November 02, 2018
				Sheet	66 of 73

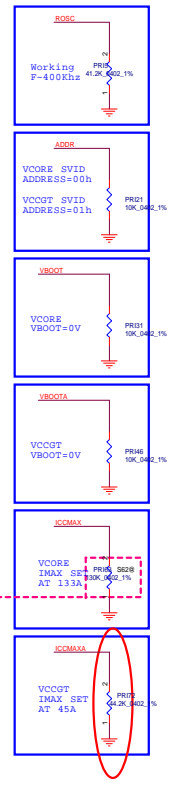
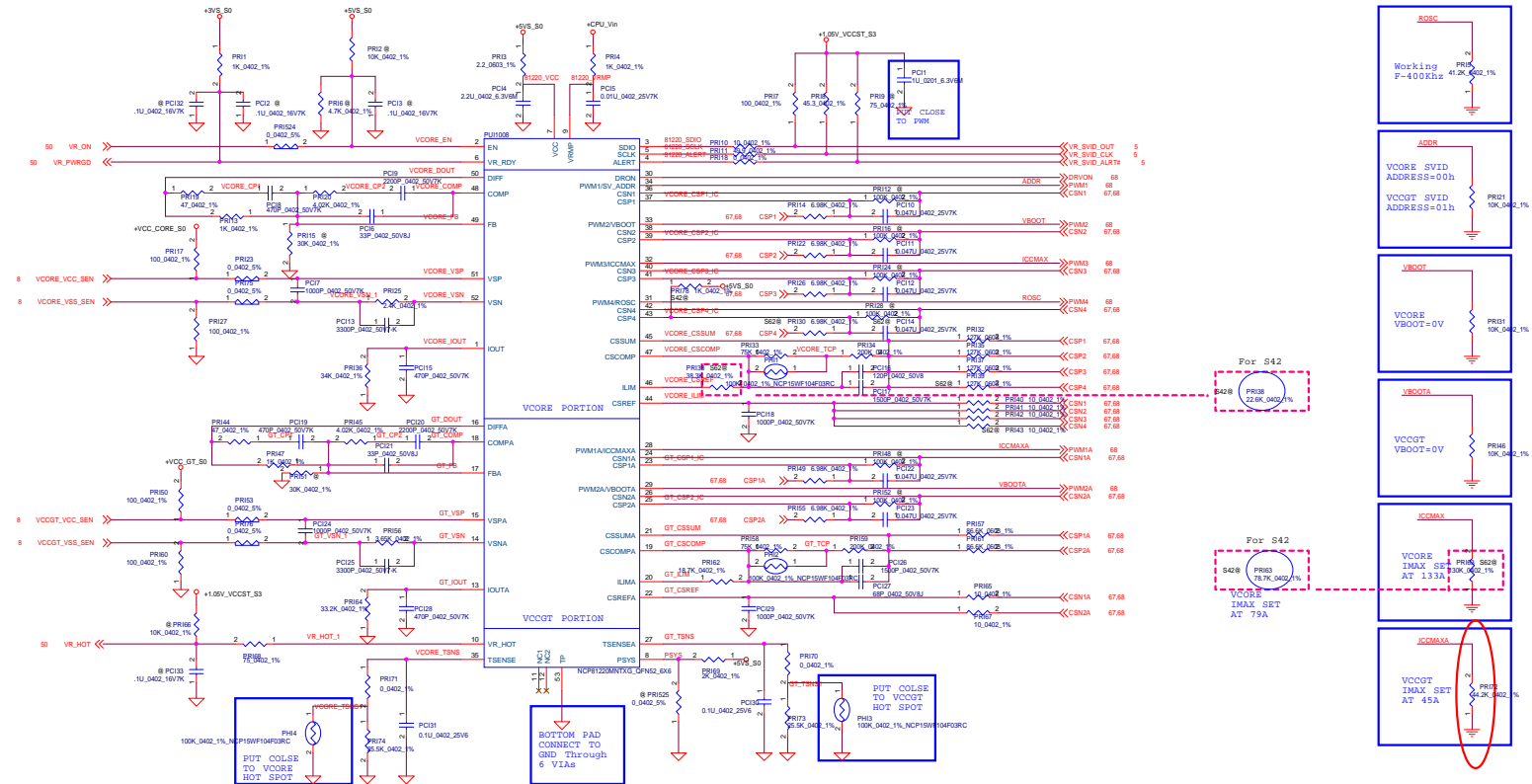


# Intel Coffeelake IMVP8 POWER CFL - S-LINE 62 35W 4+2 PHASE

S-Line 62 65W CPU power spec  
Vcore ICCMAX=133A, TDC=91A  
VccGT ICCMAX=45A, TDC=30A

# Intel Coffeelake IMVP8 POWER CFL - S-LINE 42 35W 3+2 PHASE

S-Line 42 65W CPU power spec  
Vcore ICCMAX=79A, TDC=61A  
VccGT ICCMAX=45A, TDC=30A

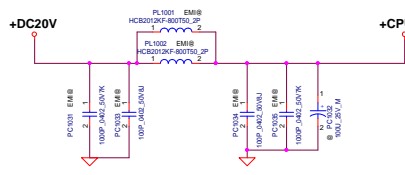


CFL - S-LINE 62 65W

<p><b>+CPU_CORE</b> TDC=51A, Ipeak=133A Fsw=350K, OCP=180A Inductor DCR=1.1mohm Output Cap. ESR=10mohm Rds H/S --&gt; typ: 4.8mohm ; max: 7mohm L/S --&gt; typ: 2.1mohm ; max: 3.3mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.255A LIR=Delta IL/Ipeak=0.394 Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =811.08 CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.03uF</p>	<p><b>+GFX_CORE</b> TDC=30A, Ipeak=45A Fsw=350K, OCP=60A Inductor DCR=1.1mohm Output Cap. ESR=10mohm Rds H/S --&gt; typ: 4.8mohm ; max: 7mohm L/S --&gt; typ: 2.1mohm ; max: 3.3mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.267A LIR=Delta IL/Ipeak=0.358 Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =577.19uF CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.69uF</p>
--	--

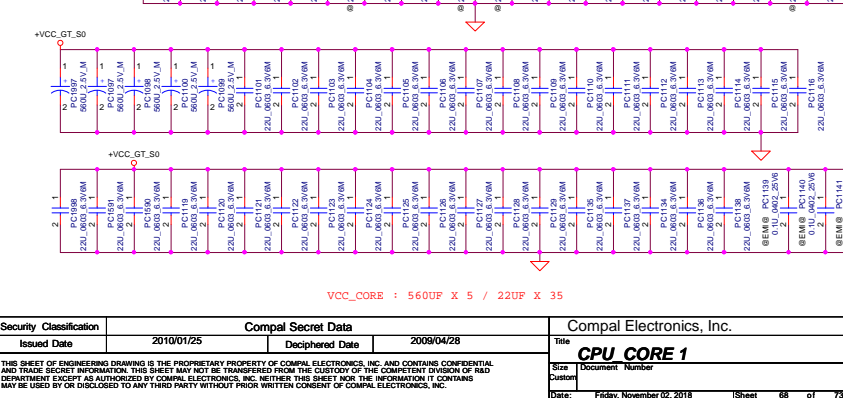
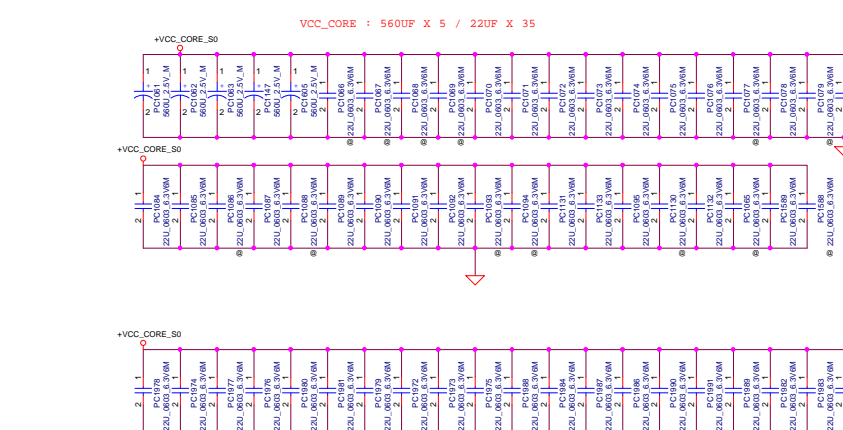
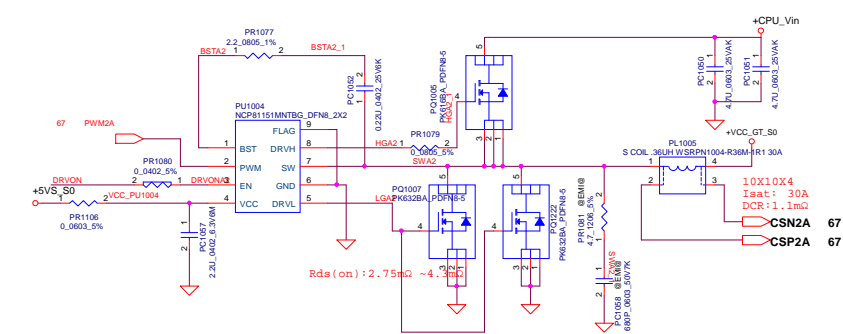
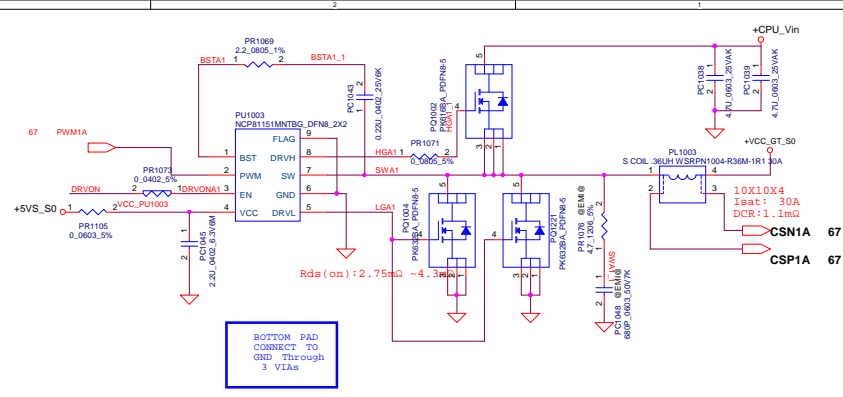
CFL - S-LINE 42 65W

<p><b>+CPU_CORE</b> TDC=61A, Ipeak=79A Fsw=350K, OCP=107A Inductor DCR=1.1mohm Output Cap. ESR=10mohm Rds H/S --&gt; typ: 4.8mohm ; max: 7mohm L/S --&gt; typ: 2.1mohm ; max: 3.3mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.255A LIR=Delta IL/Ipeak=0.394 Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =811.08 CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.03uF</p>	<p><b>+GFX_CORE</b> TDC=30A, Ipeak=45A Fsw=350K, OCP=60A Inductor DCR=1.1mohm Output Cap. ESR=10mohm Rds H/S --&gt; typ: 4.8mohm ; max: 7mohm L/S --&gt; typ: 2.1mohm ; max: 3.3mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.267A LIR=Delta IL/Ipeak=0.358 Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =577.19uF CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.69uF</p>
---	--

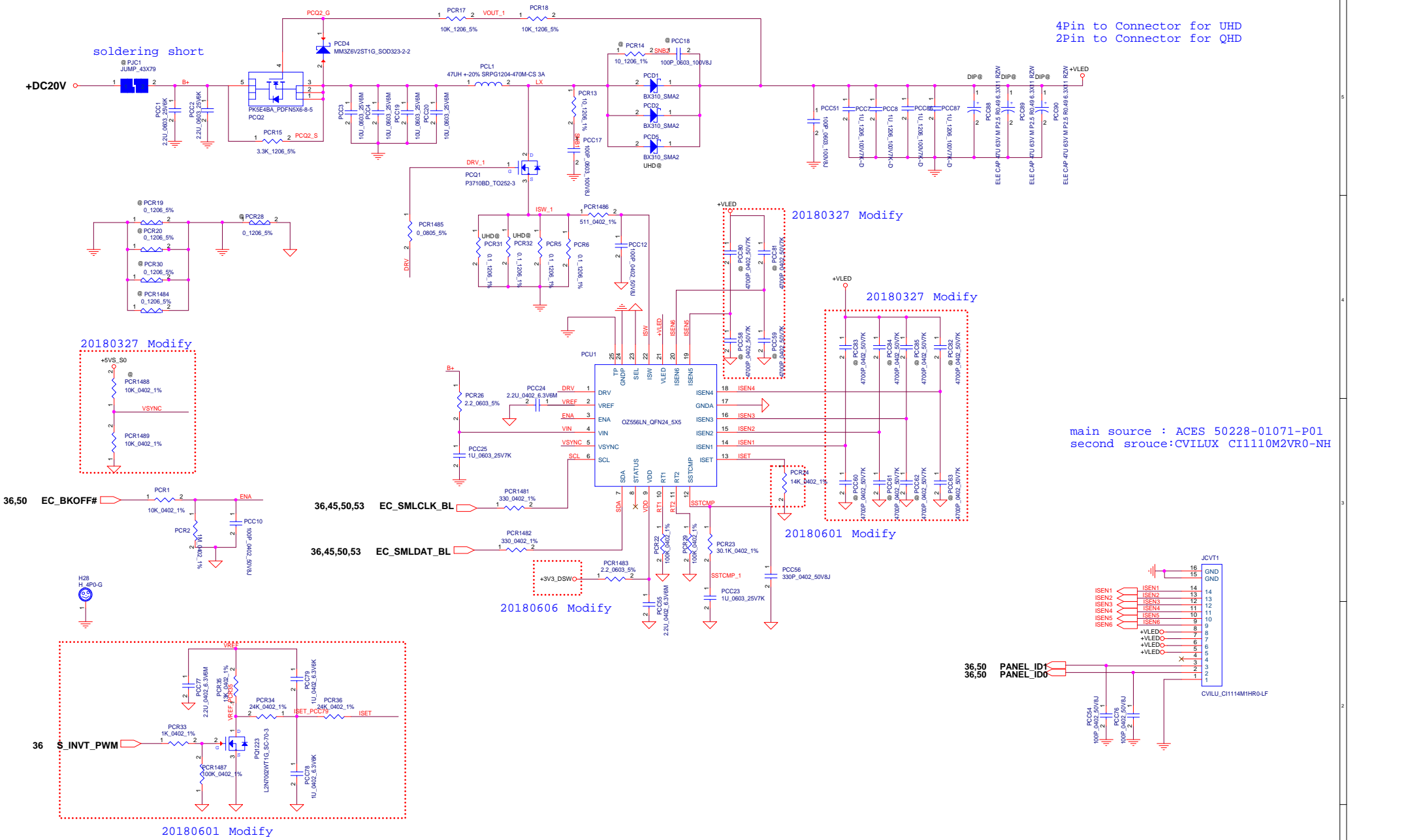


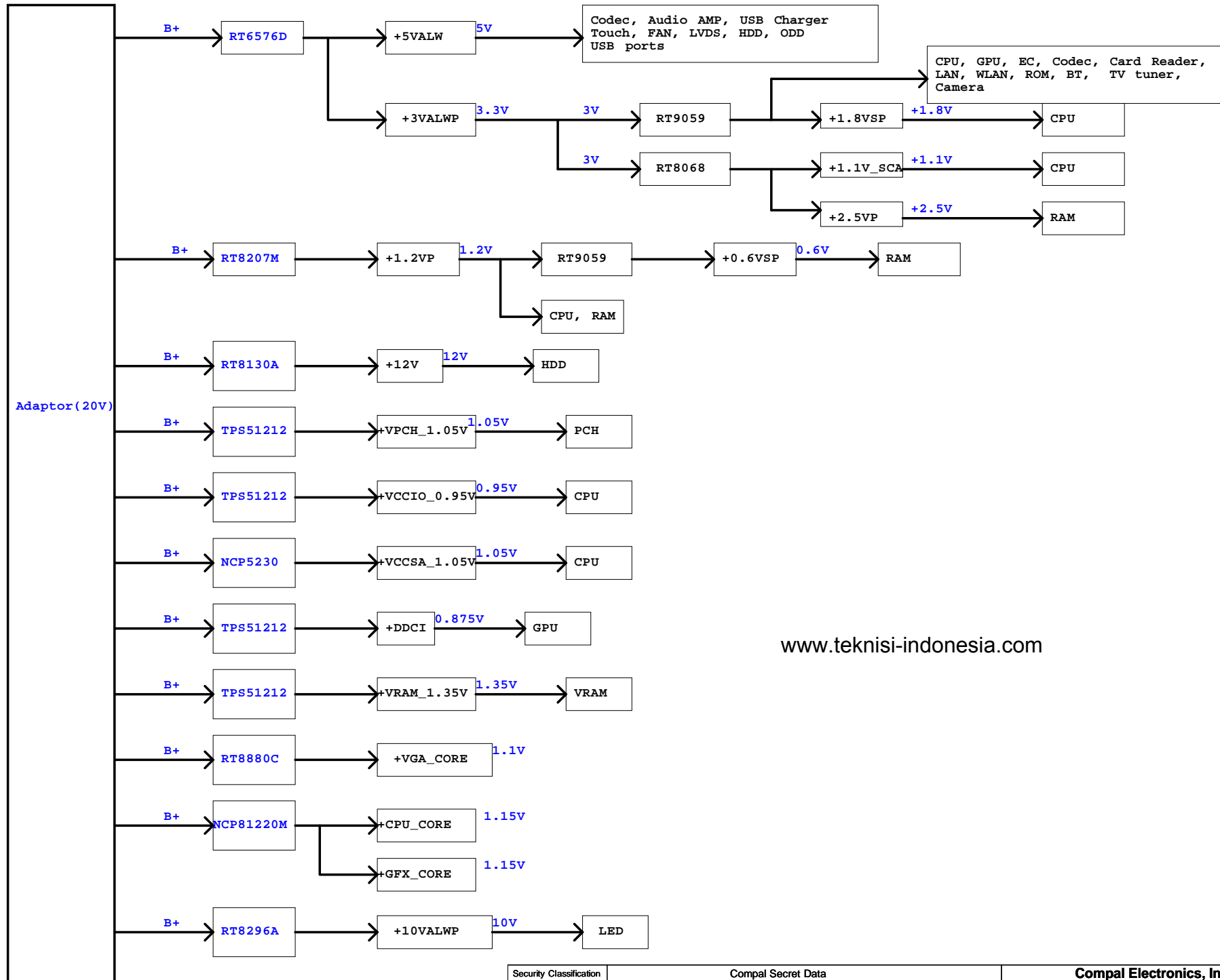
Compal Electronics, Inc.

Security Classification		Compal Secret Data		Title
Issued Date	2019/04/26	Disphered Date	2009/04/26	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				CPU CORE (INCP81220M)
Customer	Document Number	Rev	8.1	
Date	Friday, November 09, 2018	Sheet	01	75



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/01/25	Deciphered Date	2009/04/28
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT WITHOUT PRIOR APPROVAL AS AUTHORIZED BY COMPAL ELECTRONICS, INC. WHETHER THIS SHEET HAS OR HAS NOT BEEN USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Title <b>CPU CORE 1</b>
Doc. No.	Document Number	Rev.	
Issue	Issue Date	Issue By	
	Friday, November 02, 2018	Sheet	68 of 75



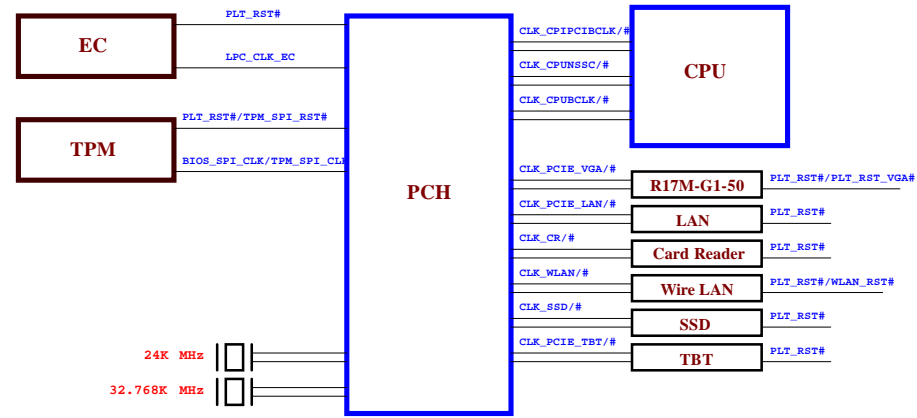
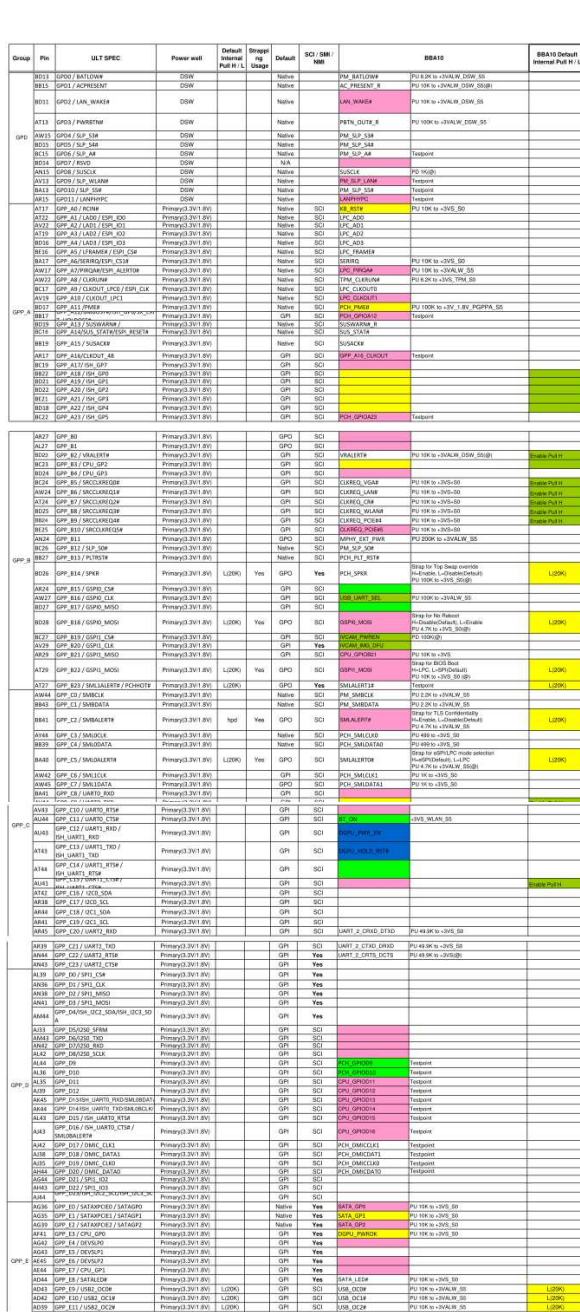


www.teknisi-indonesia.com

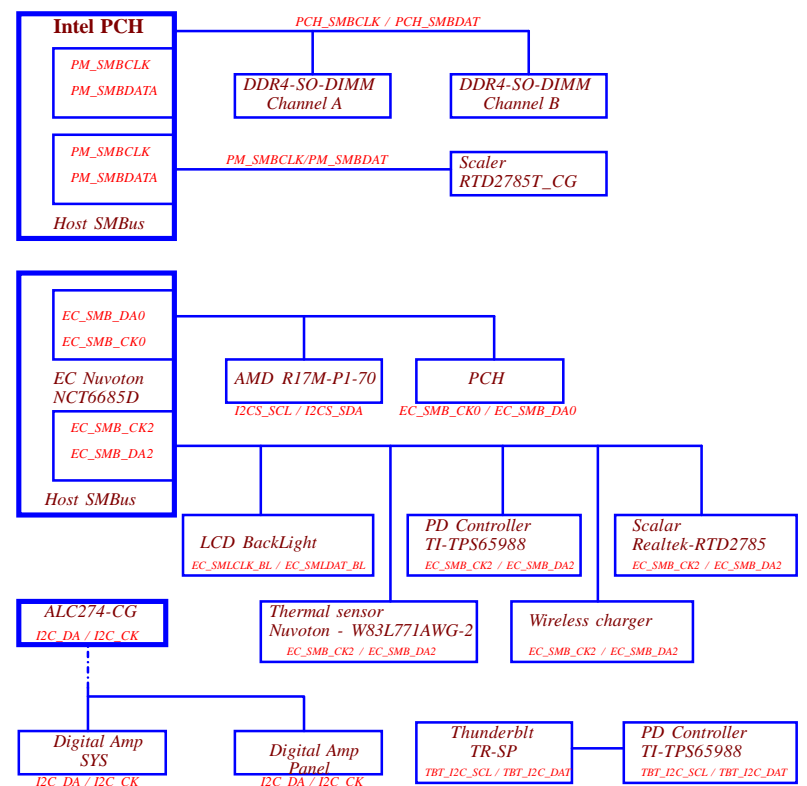
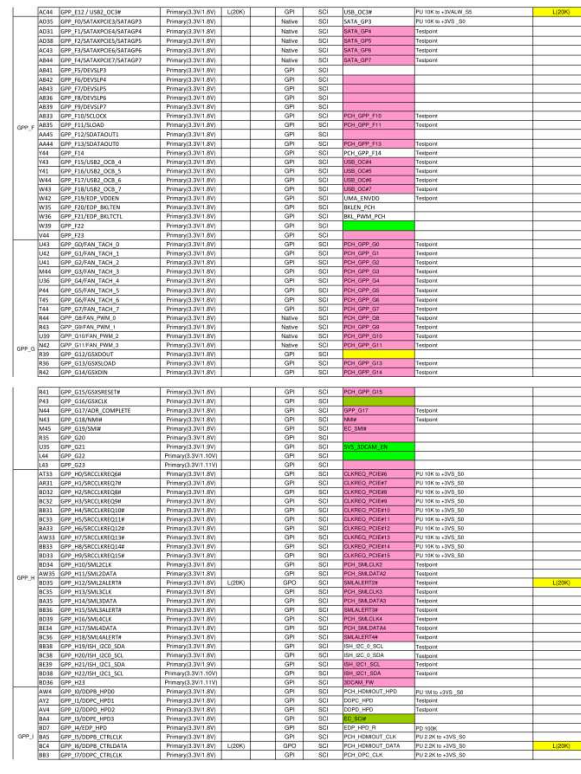
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/12/18	Deciphered Date	2013/12/18	Title	<b>Power Rail</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Rev 0.1
Date: Friday, November 02, 2018		Sheet 70 of 73			

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	05/30		SB00000ST00 ( S TR L2N7002WT1G 1N SC-70-3 ) change to SB00001CS00	Using the same material with HW
2	06/05		Change PCR34 to 4.64K	For back light current setting
3				
4				
5				

## System clock and Reset map



## SMBUS Block Diagram



Security Classification	Compul Secret Data		<b>Compul Electronics, Inc.</b> <b>GPIO Table &amp; SMBUS BD</b>	
Issued Date	2015/12/25	Deciphered Date	2015/10/02	Rev 0.1
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPUL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RAD ELECTRONICS, INC. OR ANY COMPANY CONTROLLED BY COMPUL ELECTRONICS, INC. WITHOUT THE INFORMATION IN THIS DRAWING MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPUL ELECTRONICS, INC.			<b>LA-D9S1P M/B</b>	
Date	Friday November 13, 2015		2	of 1A

**Note Color** Version change list (P,I,R. List) DVT to PVT for HW

Team	Reqs	Modified	PVT to SVT for HW	Reason for change	Date
------	------	----------	-------------------	-------------------	------

Item	Score	Pre-PVT to PVT for HW	Reason for change	Date
------	-------	-----------------------	-------------------	------

Item	Page	SIT to SVT for HW	Reason for change	Date
------	------	-------------------	-------------------	------

[illegible]